SERIALLY PROGRAMMABLE CLOCK SOURCE

ICS307-03

Description

The ICS307-03 is a dynamic, serially programmable clock source which is flexible and takes up minimal board space. Output frequencies are programmed via a 3-wire SPI port.

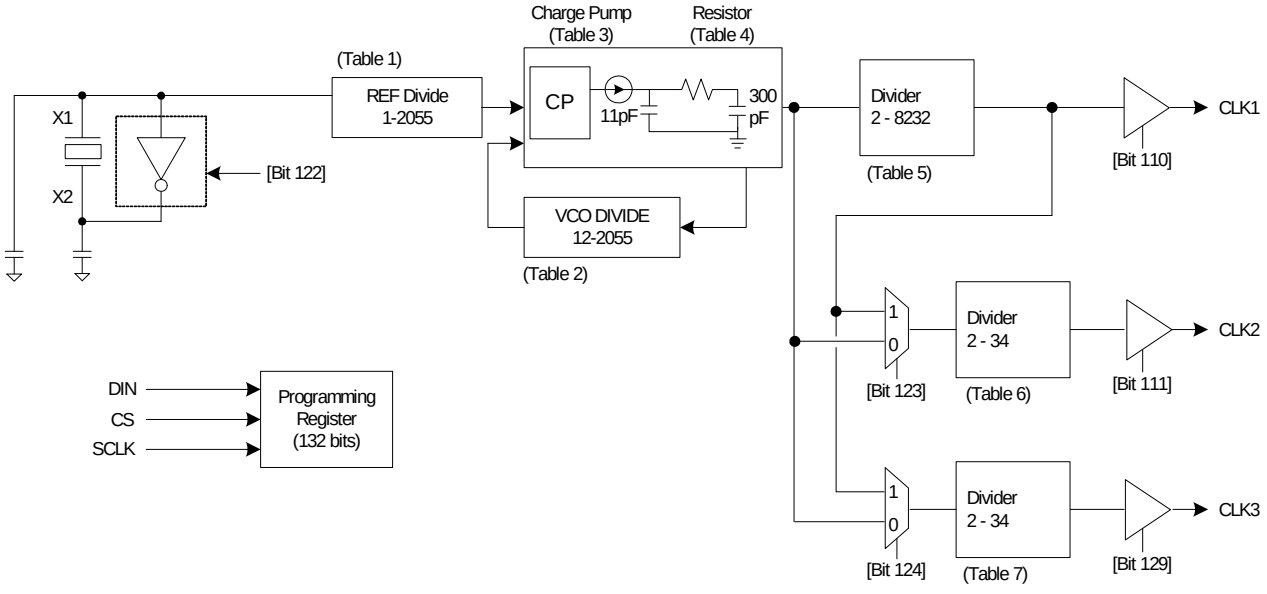
An advanced PLL coupled to an array of configurable output dividers and three outputs allows low-jitter generation of frequencies from 200 Hz to 270 MHz.

The device can be reprogrammed during operation, making it ideal for applications where many different frequencies are required, or where the output frequency must be determined at run time. Glitch-free frequency transitions, where the clock period changes slightly over many cycles, are possible.

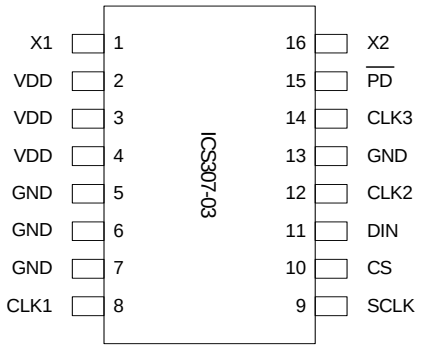
Features

- Crystal or clock reference input
- 3.3 V CMOS outputs
- Three outputs can be individually configured or shut off
- Small 16-pin TSSOP package – Pb-free, RoHS compliant
- Reprogrammable during operation
- 3-wire SPI serial interface
- Glitch-free output frequency switching
- User selectable charge pump current and damping resistor
- Power-down control via hardware pin or software control bit
- Programming word can be generated by IDT VersaClock II Software
- Directly programmable via VersaClock II Software and a Windows PC parallel port
- Industrial temperature range available

Block Diagram



Pin Assignment



16-pin TSSOP

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1	XI	Connect to input reference clock or crystal.
2	VDD	Power	Power connection for crystal oscillator.
3	VDD	Power	Power connection for PLL.
4	VDD	Power	Power connection for inputs and outputs.
5	GND	Power	Ground connection for crystal oscillator.
6	GND	Power	Ground connection for PLL.
7	GND	Power	Ground connection for inputs and outputs.
8	CLK1	Output	Clock 1 output.
9	SCLK	Input	Programming interface - Serial clock input. Internal pull-up.
10	CS	Input	Programming interface - LOAD input. Internal pull-down.
11	DIN	Input	Programming interface - Serial data input. Internal pull-up.
12	CLK2	Output	Clock 2 output.
13	GND	Power	Ground connection.
14	CLK3	Output	Clock 3 output.
15	$\overline{PD}$	Input	Crystal, PLL, and outputs are powered-down when low. Internal pull-up.
16	X2	-	Connect to crystal. Leave open if reference clock input is used.

Table 1. Input Divider

	Bits													
Divide Value	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Rule**
1	X	X	X	X	X	X	X	X	X	X	X	0	0	1+ Bit 0
2	X	X	X	X	X	X	X	X	X	X	X	0	1	1 + Bit 0
3	X	X	X	X	X	X	X	1	1	1	0	1	0	subtract 2 from the desired value, convert to binary, invert, and apply to bits 5...2 Bits [1..0] = 10
4	X	X	X	X	X	X	X	1	1	0	1	1	0	
5	X	X	X	X	X	X	X	1	1	0	0	1	0	
6	X	X	X	X	X	X	X	1	0	1	1	1	0	
7	X	X	X	X	X	X	X	1	0	1	0	1	0	
8	X	X	X	X	X	X	X	1	0	0	1	1	0	
9	X	X	X	X	X	X	X	1	0	0	0	1	0	
10	X	X	X	X	X	X	X	0	1	1	1	1	0	
11	X	X	X	X	X	X	X	0	1	1	0	1	0	
12	X	X	X	X	X	X	X	0	1	0	1	1	0	
13	X	X	X	X	X	X	X	0	1	0	0	1	0	
14	X	X	X	X	X	X	X	0	0	1	1	1	0	
15	X	X	X	X	X	X	X	0	0	1	0	1	0	
16	X	X	X	X	X	X	X	0	0	0	1	1	0	
17	X	X	X	X	X	X	X	0	0	0	0	1	0	
18	0	0	0	0	0	0	0	1	0	1	0	1	1	subtract 8 from the desired divide value, convert to binary, and apply to bits 11...2 Bits [1..0] = 11
19	0	0	0	0	0	0	0	1	0	1	1	1	1	
20	0	0	0	0	0	0	0	1	1	0	0	1	1	
21	0	0	0	0	0	0	0	1	1	0	1	1	1	
⋮														
2054	1	1	1	1	1	1	1	1	1	1	0	1	1	
2055	1	1	1	1	1	1	1	1	1	1	1	1	1	

Table 2. VCO Divider

	Bits											
Divide Value	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**Rule**
12	0	0	0	0	0	0	0	0	1	0	0	subtract 8 from the desired divide value, convert to binary, and apply to bits 23...13
13	0	0	0	0	0	0	0	0	1	0	1	
14	0	0	0	0	0	0	0	0	1	1	0	
⋮												
2054	1	1	1	1	1	1	1	1	1	1	0	
2055	1	1	1	1	1	1	1	1	1	1	1	

Table 3. Charge Pump Current

	Bits					
Charge Pump Current (μA)	**93**	**92**	**91**	**128**	**127**	**Rule**
1.25	1	1	1	0	0	Icp = ([128...127]+1)*1.25μA*([$\overline{93}$ $\overline{92}$ $\overline{91}$] + 1)
2.5	1	1	0	0	0	
2.5	1	1	1	0	1	
3.75	1	0	1	0	0	
3.75	1	1	1	1	0	
5	1	0	0	0	0	
5	1	1	0	0	1	
5	1	1	1	1	1	
6.25	0	1	1	0	0	
7.5	0	1	0	0	0	
7.5	1	1	0	1	0	
7.5	1	0	1	0	1	
8.75	0	0	1	0	0	
10	0	0	0	0	0	
10	1	0	0	0	1	
10	1	1	0	1	1	
11.25	1	0	1	1	0	
12.5	0	1	1	0	1	
15	1	0	0	1	0	
15	0	1	0	0	1	
15	1	0	1	1	1	
17.5	0	0	1	0	1	
18.75	0	1	1	1	0	
20	0	0	0	0	1	
20	1	0	0	1	1	
22.5	0	1	0	1	0	
25	0	1	1	1	1	
26.25	0	0	1	1	0	
30	0	0	0	1	0	
30	0	1	0	1	1	
35	0	0	1	1	1	
40	0	0	0	1	1	

Table 4. Loop Filter Resistor

	Bits	
Resistor Value	**90**	**89**
64 k	0	0
52 k	0	1
16 k	1	0
4 k	1	1

Table 5. Output Divider for Output 1

Divide Value	Bits 109	108	107	106	105	104	103	102	101	100	99	98	97	96	95	Rule
2	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0	
3	X	X	X	X	X	X	X	X	X	X	X	0	0	0	1	
4	X	X	X	X	X	X	X	X	X	X	X	1	0	0	0	
5	X	X	X	X	X	X	X	X	X	X	X	X	0	1	0	
6	X	X	X	X	X	X	X	X	X	X	X	1	0	0	1	
7	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	
8	X	X	X	X	X	X	X	1	1	1	0	1	1	0	0	apply Rule from Divide Values 14-37
9	X	X	X	X	X	X	X	X	X	X	0	1	0	1	1	
10	X	X	X	X	X	X	X	1	1	0	1	1	1	0	0	apply Rule from Divide Values 14-37
11	X	X	X	X	X	X	X	X	X	X	1	0	0	1	1	
12	X	X	X	X	X	X	X	1	1	0	0	1	1	0	0	apply Rule from Divide Values 14-37
13	X	X	X	X	X	X	X	X	X	X	1	1	0	1	1	
14	X	X	X	X	X	X	X	1	0	1	1	1	1	0	0	subtract 6 from the desired divide value, convert to binary, invert, and apply to bits 102..98 set bits [97..95] = 100
15	X	X	X	X	X	X	X	1	0	1	1	0	1	0	0	
36	X	X	X	X	X	X	X	0	0	0	0	1	1	0	0	
37	X	X	X	X	X	X	X	0	0	0	0	0	1	0	0	
38	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	output divide = ((([109..101]+3)*2)+[$\overline{98}$])*2^[100..99] set bits [95..97] = 101
39	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	
⋮	(increments of 1)															set bits [95..97] = 101 †
1029	1	1	1	1	1	1	1	1	1	0	0	0	1	0	1	(† this Rule applies to Divide Values 38-8232)
1030	0	1	1	1	1	1	1	1	0	0	1	0	1	0	1	
1032	0	1	1	1	1	1	1	1	1	0	1	1	1	0	1	
⋮	(increments of 2)															
2056	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	
2058	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	
2060	0	1	1	1	1	1	1	1	0	1	0	0	1	0	1	
2064	0	1	1	1	1	1	1	1	1	1	0	1	1	0	1	
⋮	(increments of 4)															
4112	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	
4116	1	1	1	1	1	1	1	1	1	1	0	0	1	0	1	
4120	0	1	1	1	1	1	1	1	0	1	1	0	1	0	1	
4128	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	
⋮	(increments of 8)															
8224	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	
8232	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	

Table 6. Output Divider for Output 2

	Bits					
Divide Value	**117**	**116**	**115**	**114**	**113**	**Rule**
2	1	1	1	1	0	output divide = ([$\overline{117}$..$\overline{114}$]+2)*2^[113])
4	1	1	1	1	1	
6	1	1	1	0	1	
8	1	1	0	1	1	
10	1	1	0	0	1	
12	1	0	1	1	1	
14	1	0	1	0	1	
16	1	0	0	1	1	
18	1	0	0	0	1	
20	0	1	1	1	1	
22	0	1	1	0	1	
24	0	1	0	1	1	
26	0	1	0	0	1	
28	0	0	1	1	1	
30	0	0	1	0	1	
32	0	0	0	1	1	
34	0	0	0	0	1	

Table 7. Output Divider for Output 3

	Bits					
Divide Value	**121**	**120**	**119**	**118**	**94**	**Rule**
2	1	1	1	1	0	output divide = ([$\overline{121}$..$\overline{118}$]+2)*2^[94])
4	1	1	1	1	1	
6	1	1	1	0	1	
8	1	1	0	1	1	
10	1	1	0	0	1	
12	1	0	1	1	1	
14	1	0	1	0	1	
16	1	0	0	1	1	
18	1	0	0	0	1	
20	0	1	1	1	1	
22	0	1	1	0	1	
24	0	1	0	1	1	
26	0	1	0	0	1	
28	0	0	1	1	1	
30	0	0	1	0	1	
32	0	0	0	1	1	
34	0	0	0	0	1	

Table 8. Miscellaneous Control Bits

Bit	Function
24~88	Reserved—set to 0
110	OE1—set to 1 to enable CLK1
111	OE2—set to 1 to enable CLK2
112	1 = Normal Operation, 0 = power down feedback counter, charge pump and VCO
122	Crystal Input = 1, Clock Input = 0
123	Selects source for CLK2 (see block diagram)
124	Selects source for CLK3 (see block diagram)
125	Reserved—set to 0
126	Reserved—set to 0
129	OE3—set to 1 to enable CLK3
130	Reserved—set to 0
131	Reserved—set to 0

External Components

The ICS307-03 requires a minimum number of external components for proper operation.

Decoupling Capacitors

TheICS307-03 requires 0.01µF decoupling capacitors to be connected between each VDD pin and the Ground Plane. The 0.01µF capacitors must be placed as close to the ICS307-03's power pins as possible to minimize lead inductance.

Output Termination

The ICS307-03 has advanced output pads that allows the device to achieve very high speed (270 MHz) operation with single ended clock outputs. The clock outputs on the ICS307-03 are designed to be directly connected to a 50 Ohm transmission line without the need for any series resistors.

Crystal Selection

A parallel resonant, fundamental mode crystal with a load (correlation) capacitance of 12 pF should be used. For crystals with a specified load capacitance greater than 12 pF, additional crystal capacitors may be connected from each of the pins X1 and X2 to ground as shown in the Block Diagram on page 1. The value (in pF) of these crystal caps should be = $(C_L-12)*2$, where C_L is the crystal load capacitance in pF.

For a single ended clock input, connect it to X1 and leave X2 unconnected with no capacitors on either pin.

Initial Output Frequency

ICS307-03 on-chip registers are initially configured to provide a 1x output clock on the CLK1 output, and 0.5x clock on CLK2 and CLK3. The output frequency will be the same as the input clock or crystal for input frequencies from 10 - 50 MHz. This is useful when the ICS307-03 needs to provide an initial system clock at power-up.

Determining and Controlling the Output Frequency with VersaClock™ II

The ICS307-03 is directly supported by the IDT provided software called VersaClock II. Complete programming words for this device can be calculated on any Windows PC by running the VersaClock II software and simple inputting desired input and output frequencies. Once the software generates an appropriate programming word, it may then be either copied to the Windows clipboard or even directly programmed into the ICS307-03 via the host computers parallel port.

For more information on VersaClock II, please visit www.icst.com or send an e-mail to ics-mk@icst.com.

Manually Determining the Output Frequency

The user has full control over the desired output frequency as long as it is operated within the limits shown in the AC Electrical Characteristics.

The output of the ICS307-03 can be determined by the following equation:

$$CLK1Frequency = InputFrequency \cdot \frac{V}{R \cdot OD}$$

Where:
VCO Divider (V) = 12 to 2055
Reference Divider Word (R) = 1 to 2055
Output Divider = values in tables 5, 6, 7

Default Register Values

At power-up, the registers are set to:
ref divide = 5
VCO divide = 50
output divide = 10 (CLK1)
output divide = 2 (CLK2)
output divide = 2 (CLK3)
bit 123, 124 = 1
ICP = 3.75 µA
R = 16k

Default programming word is:
0x31FFDFFEE3BFFFFFFFFFFFFFFF055FF2

Also, the following operating ranges should be observed.

$$VCOmin < InputFrequency \cdot \frac{V}{R} < VCOmaxfreq$$

$$20kHz < \frac{Input\ Frequency}{R} < 100MHz$$

To determine the best combination of VCO, reference, and output dividers, please use the VersaClock II software mentioned above.

Programming Interface

The dynamic register within the ICS307-03 controls the entire device and may be reprogrammed any time after power is properly applied. If V or R values are changed, the frequency will transition smoothly to the new value without glitches or short cycles. However, changing any divider or mux in the output signal path may generate a glitch.

The register is 132 bits in length and accepts the MSB first. The SCLK signal latches the current data bit value in the rising edge. It latches the most recently shifted 132 bit values into the control register of device whenever CS is high. Care must be taken to ensure that CS is always low until the system is ready to load in a new register value and that SCLK is never toggled high when CS is high.

The register can be programmed any time after power is applied, even while in power-down (pin 15 or bit 112 held low) with the waveform and timing shown below:.

Figure 2: ICS307-03 Programming Timing Diagram

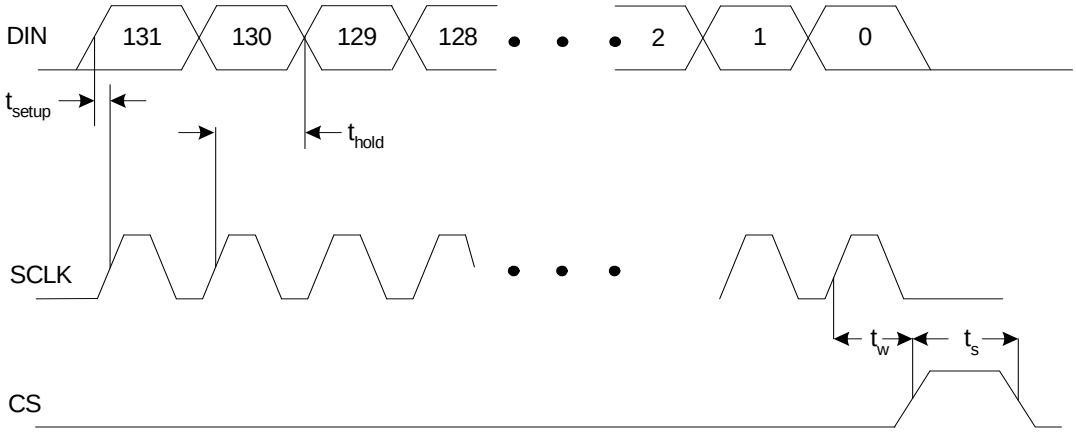


Table 8: AC Parameters for Programming the ICS307-03

Parameter	Condition	Min.	Max.	Units
t_{SETUP}	Setup time	2.5		ns
t_{HOLD}	Hold time after SCLK	2.5		ns
t_W	Data wait time	2.5		ns
t_S	Strobe pulse width	10		ns
	SCLK Frequency		200	MHz

Programming with VersaClock Software

The VersaClock II Software not only generates the programming word for the user, it can also be used to program the device via the host computer's parallel port. Demonstration boards are available from IDT that allows the VersaClock II S/W to directly connect the ICS307-03 to a Windows based PC's DB-25 parallel port connector and programmed simply by pressing the "Program Part" button.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS307-03. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.

Exposure to absolute maximum rating conditions for extended periods can affect product reliability.

Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	5 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

DC Electrical Characteristics

VDD=3.3 V ±0.3 V, Ambient temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		3.6	V
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 4 mA			0.4	V
Output High Voltage, CMOS level	V_{OH}	I_{OH} = -6.5 mA	VDD-0.4			V
Tri-state Output Leakage				1		µA
Operating Supply Current	IDD	27 MHz crystal No load, 100 MHz out, all outputs enabled		24		mA
Short Circuit Current		CLK outputs		±60		mA
Input Capacitance	C_{IN}			4		pF
On-Chip Pull-up Resistor	R_{PU}			240		kΩ
On-Chip Pull-down Resistor	R_{PD}			100		kΩ

AC Electrical Characteristics

VDD = 3.3 V ±0.3 V, Ambient Temperature 0 to +70° C, unless stated otherwise

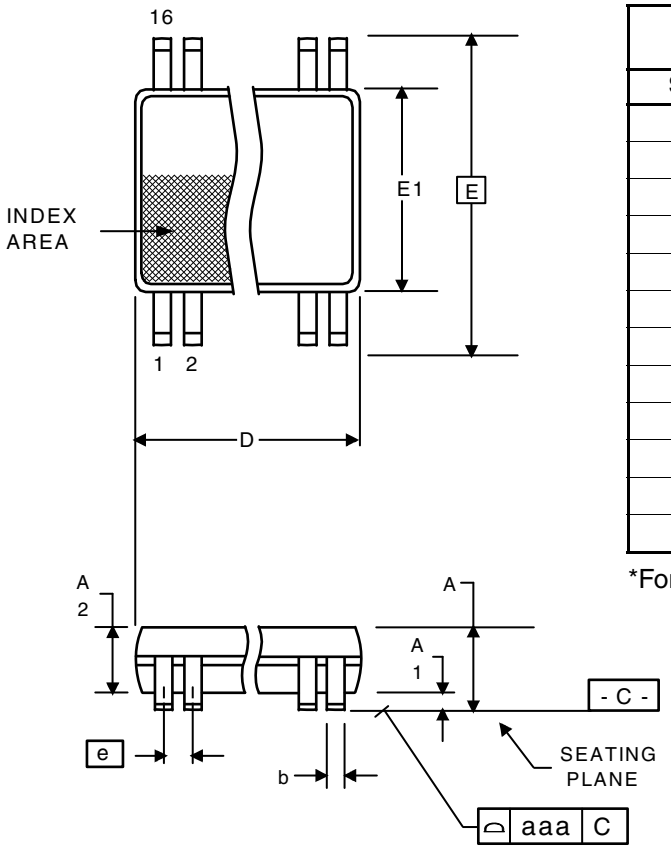
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}	Fundamental crystal	3		27	MHz
		Clock	0.1		300	MHz
Clock Output Frequency	F_{OUT}	5 pF load	0.0002		270	MHz
		15 pF load	0.0002		200	MHz
Output Clock Rise/Fall Time	t_R, t_F	20 to 80% (5 pF load)		1.5		ns
Output Clock Duty Cycle		Output Divides <> 3	45	49-51	55	%
		Output Divide = 3	40		60	%
Frequency Transition time		STROBE high to CLK out		3	10	ms
One Sigma Clock Period Jitter		Note 2		50		ps
Maximum Absolute Jitter	t_{ja}	Deviation from mean, Note 2		±120		ps
VCO Frequency	VCO_F		100		730	MHz
Divider 1 Input		Output divider 1 = 2 (5 pF load)			540	MHz
		Output divider 1 = 2 (15 pF load)			400	MHz
		Output divider 1 = 3 (5 pF load)			720	MHz
		Output divider 1 = 3 (15 pF load)			600	MHz
		Output divider 1 = 38 ~ 1029			570	MHz
		All other Output Divider 1 values			730	MHz
Divider 2 and 3 Inputs		Output divider 2, 3 = 2 (5 pF load)			540	MHz
		Output divider 2, 3 = 2 (15 pF load)			400	MHz
		Output divider 2, 3=12			440	MHz
		Output divider 2, 3 = 16, 24, 28 and 32			500	MHz
		All other Output Divider 2 & 3 values			730	MHz

Note 1: Measured with 15 pF load.

Note 2: Jitter performance will change depending on configuration settings.

Package Outline and Package Dimensions (16-pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



	Millimeters		Inches*	
Symbol	Min	Max	Min	Max
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

*For reference only. Controlling dimensions in mm.

Ordering Information

Part / Order Number	Marking	Shipping packaging	Package	Temperature
307G-03LF	307G03LF	Tubes	16-pin TSSOP	0 to +70° C
307G-03LFT	307G03LF	Tape and Reel	16-pin TSSOP	0 to +70° C
307GI-03LF	307GI03L	Tubes	16-pin TSSOP	-40 to +85° C
307GI-03LFT	307GI03L	Tape and Reel	16-pin TSSOP	-40 to +85° C

"LF" suffix to the part number denotes Pb-Free configuration, RoHS compliant.

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