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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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H5N5004PL

Silicon N Channel MOS FET High Speed Power Switching

RENESAS

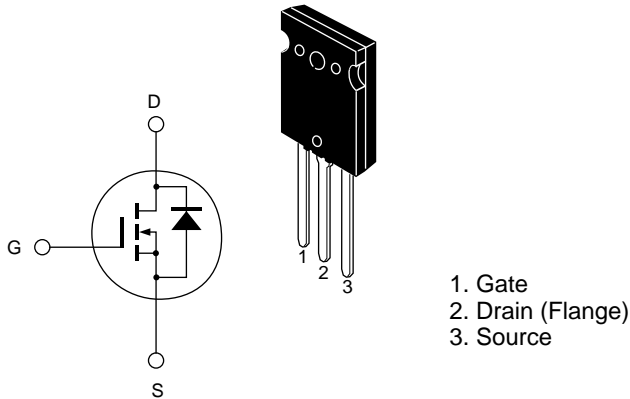
ADE-208-1381 (Z)
Target Specification 1st. Edition
Mar. 2001

Features

- Low on-resistance: $R_{DS(on)} = 0.09 \Omega$ typ.
- Low leakage current: $IDSS = 10 \mu A$ max (at $V_{DS} = 500 V$)
- High speed switching: $t_f = 280 ns$ typ (at $V_{GS} = 10 V$, $V_{DD} = 250 V$, $I_D = 25 A$)
- Low gate charge: $Q_g = 220 nC$ typ (at $V_{DD} = 400 V$, $V_{GS} = 10 V$, $I_D = 50 A$)
- Avalanche ratings
- Built-in fast recovery diode: $t_{rr} = 190 ns$ typ

Outline

TO-3PL



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	50	A
Drain peak current	$I_{D (pulse)}^{Note1}$	200	A
Body-drain diode reverse drain current	I_{DR}	50	A
Body-drain diode reverse drain peak current	$I_{DR (pulse)}^{Note1}$	200	A
Avalanche current	I_{AP}^{Note3}	15	A
Channel dissipation	P_{ch}^{Note2}	250	W
Channel to case Thermal Impedance	θ_{ch-c}	0.5	°C/W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$

2. Value at $T_c = 25^\circ C$

3. $T_{ch} \leq 150^\circ C$

Electrical Characteristics (Ta = 25°C)

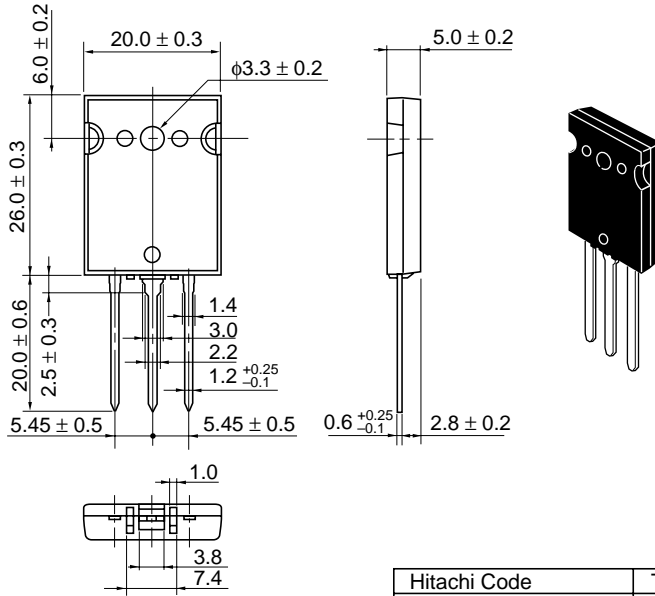
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 500 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.09	0.11	Ω	$I_D = 25 \text{ A}, V_{GS} = 10 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	27	45	—	S	$I_D = 25 \text{ A}, V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	7630	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	C_{oss}	—	770	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	160	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	90	—	ns	$I_D = 25 \text{ A}$
Rise time	t_r	—	340	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	370	—	ns	$R_L = 10 \Omega$
Fall time	t_f	—	280	—	ns	$R_g = 10 \Omega$
Total gate charge	Q_g	—	220	—	nC	$V_{DD} = 400 \text{ V}$
Gate to source charge	Q_{gs}	—	30	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	110	—	nC	$I_D = 50 \text{ A}$
Body-drain diode forward voltage	V_{DF}	—	0.98	1.5	V	$I_F = 50 \text{ A}, V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	190	—	ns	$I_F = 50 \text{ A}, V_{GS} = 0$
Body-drain diode reverse recovery charge	Q_{rr}	—	1.3	—	μC	$diF/dt = 100 \text{ A}/\mu\text{s}$

Note: 4. Pulse test

Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	TO-3PL
JEDEC	—
EIAJ	—
Mass (reference value)	9.9 g

Cautions

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