FUJI Power Supply Control IC

Power Factor Correction

FA5500AP/AN
FA5501AP/AN

November `02
Fuji Electric Co., Ltd.
Matsumoto Factory

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Note

- Parts tolerance and characteristics are not defined in all application described in this Data book. When design an actual circuit for a product, you must determine parts tolerances and characteristics for safe and economical operation.

1. Description

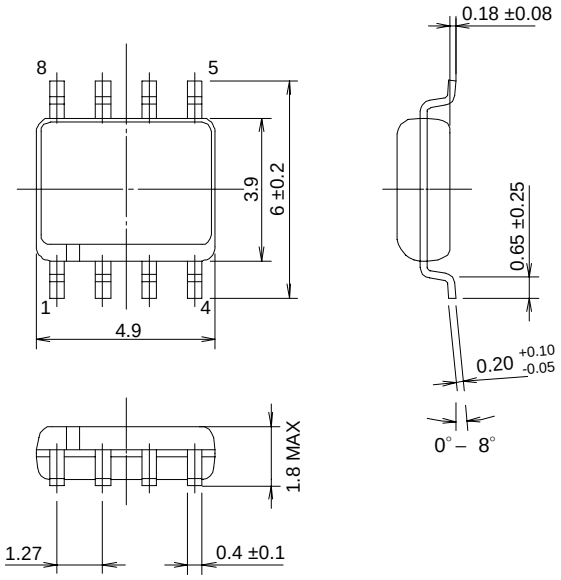
FA5500A/FA5501A are control ICs for a power factor correction converter using critical conduction mode of operation. This IC uses a CMOS device with high dielectric strength (30V) to implement low power consumption. These ICs contain compensated current sense comparator for light load and open/short protection at feedback (FB) pin. Compensated current sense comparator for light load keeps output voltage constant from no-load to full-load. Open/short protection at FB pin stops output pulses when voltage divider to detect output voltage becomes fault.

2. Features

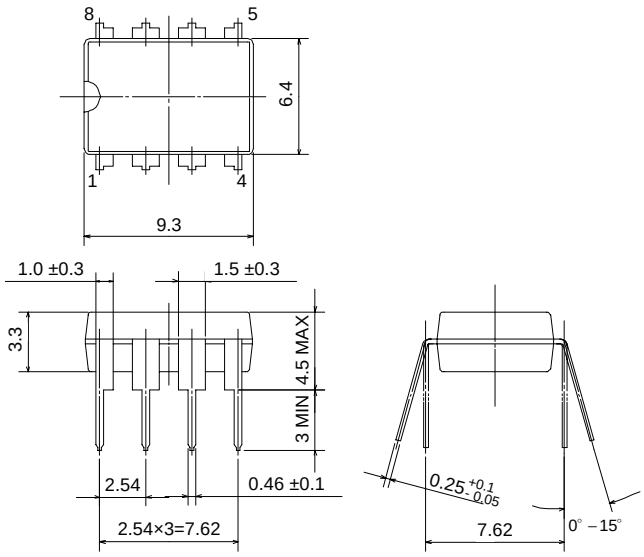
- Low current consumption by CMOS process
  Start-up : 20μA(max.), Operating : 1mA(typ.)
- Drive circuit for connecting a power MOSFET directly
- Output peak current, source : 500mA, sink : 1000mA
- Compensated current sense comparator for light load
- Open/short protection at feedback (FB) pin
- Undervoltage Lockout
  FA5500A: 11.5V ON / 9V OFF FA5501A:13V ON / 9V OFF
- Overvoltage protection
- Restart timer
- Package: DIP-8 / SOP-8

3. Outline

SOP-8



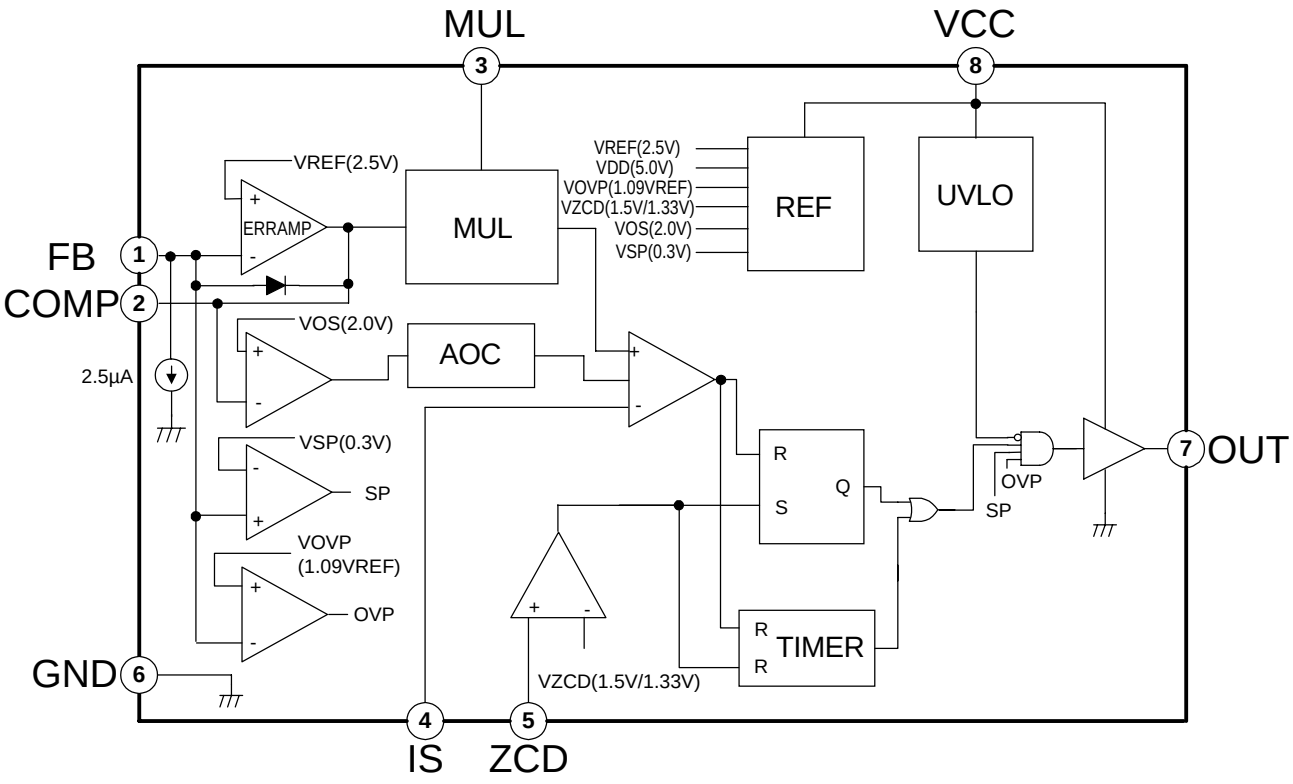
DIP-8



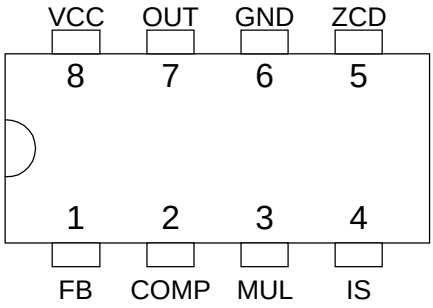
4. Types of FA5500A/01A

Type	Startup Threshold	Package
FA5500AP	11.5V(typ.)	DIP-8
FA5500AN	11.5V(typ.)	SOP-8
FA5501AP	13V(typ.)	DIP-8
FA5501AN	13V(typ.)	SOP-8

5. Block diagram



6. Pin assignment



Pin No.	Pin symbol	Function	Description
1	FB	Voltage Feedback Input	Input for monitoring PFC output voltage
2	COMP	Compensation	Output of error amplifier
3	MUL	Multiplier Input	Input of multiplier for monitoring sinusoidal waveform
4	IS	Current Sense Input	Input for sensing MOSFET current signal
5	ZCD	Zero Current Detect Input	Input for detecting that the inductor current reaches zero
6	GND	Ground	Ground
7	OUT	Output	Output for direct driving a power MOSFET
8	VCC	Power Supply	Power supply for IC

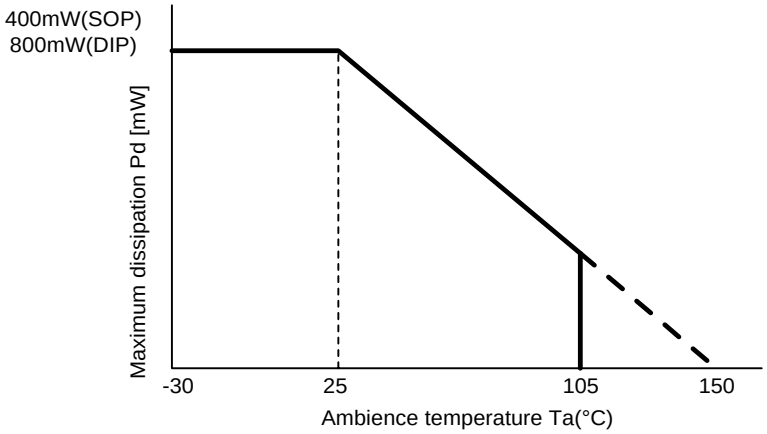
7. Ratings and characteristics

The contents are subject to change without notice. When using a product, be sure to obtain the latest specifications.

(1) Absolute Maximum Ratings

Item			Symbol	Ratings	Unit
Total Power Supply and Zener Current			Icc+Iz	30	mA
Supply Voltage	Zener Clamp (Icc+Iz<30mA)		Vcc	Self Limiting	V
Output Current		Sink Source	Io	+1000 -500	mA mA
Input voltage(IS,MUL,FB)			Vin	-0.3 to 5	V
Zero Current Detect Input High State Forward Current Low State Reverse Current			Iin	 -50 10	 mA
Power dissipation		DIP-8	Pd1	800	mW
		SOP-8	Pd2	400	mW
Operating Ambient Temperature			Ta	-30 to +105	°C
Operating Junction Temperature			Tj	+150	°C
Storage Temperature			Tstg	-55 to +150	°C

Maximum dissipation curve



(2) Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	10	12	28	V
ZCD pin current	Izcd			±3	mA

(3)Electrical Characteristics (Unless otherwise specified, Ta=25°C and Vcc=12V)

ERROR AMPLIFIER(FB,COMP Pin)

Item	Symbol	Condition	Min	Typ	Max	Unit
Voltage Feedback Input Threshold	Vfb	Ta=25°C	2.465	2.500	2.535	V
Line Regulation	Regline	Vcc=12V to 28V Ta=25°C	-50	-20	-	mV
Temperature stability	VdT	Ta=-30°C to +105°C		±0.5		mV/°C
Transconductance	Gm	Ta=25°C	70	90	120	µmho
Output Current	Io	Source(Vfb=2.3V) Sink(Vfb=2.7V)	- -	10 10	- -	µA

OVERVOLTAGE COMPARATER (FB Pin)

Item	Symbol	Condition	Min	Typ	Max	Unit
Input Threshold	Vthovp		1.075Vfb	1.09Vfb	1.105Vfb	V

FB SHORT COMPARATOR(FB Pin)

Item	Symbol	Condition	Min	Typ	Max	Unit
Input Threshold	Vthsht		0.1	0.3	0.5	V
Pulldown Current	Ifb		0.5	2.5	5	µA

MULTIPLIER(COMP,MUL Pin)

Item	Symbol	Condition	Min	Typ	Max	Unit
Input Threshold Pin2(COMP)	Vthcomp		1.79	2.04	-	V
Dynamic Input Voltage Range Pin3(MUL) Pin2(COMP)	 Vpin3 Vpin2		 0 to 2.5 Vthcomp to Vthcomp +1.0	 0 to 3.5 Vthcomp to Vthcomp +1.5	-	V
Gain	K	Vpin3=0.5V Vpin2=Vthcomp +1.0V	0.53	0.75	0.97	1/V

K=Pin4Threshold/{Vpin3(Vpin2-Vthcomp)}

ZERO CURRENT DETECTOR (ZCD Pin)

Item	Symbol	Condition	Min	Typ	Max	Unit
Input Threshold Voltage	Vthzcd	Vin increasing	1.33	1.50	1.87	V
Hysteresis	Vh	Vin decreasing	100	170	300	mV
Input Clamp Voltage “H” state “L” state	 Vih Vil	 Idet=+3.0mA Idet=-3.0mA	 7.0 0.3	 7.6 0.6	 - 1.0	V

CURRENT SENSE COMPARATOR (IS Pin)

Item	Symbol	Condition	Min	Typ	Max	Unit
Maximum Current Sense Input Threshold	Vthis	Vpin1=1.0V Vpin3=3.0V	1.3	1.5	1.8	V
Delay to Output	Tphl		-	170	400	ns

DRIVE OUTPUT (OUT Pin)

Item	Symbol	Condition	Min	Typ	Max	Unit
Output Voltage Low State	Vol	Vcc=12V Isink=200mA	-	1.2	3.3	V
Output Voltage High State	Voh	Vcc=12V Isouce=200mA	7.8	8.4		V
Output Voltage Rise Time	Tr	CL=1.0nF	-	50	120	ns
Output Voltage Fall Time	Tf	CL=1.0nF	-	25	100	ns

RESTART TIMER

Item	Symbol	Condition	Min	Typ	Max	Unit
Restart Time Delay	Tdly		100	200	-	µs

UNDERVOLTAGE LOCKOUT (VCC Pin)

Item	Symbol	Condition	Min	Typ	Max	Unit
Startup Threshold	Von	FA5500A	10	11.5	13	V
		FA5501A	11.5	13	14.5	V
Minimum Operating Voltage After Turn-On	Voff		8	9	10	V
Hysteresis	Vhysvcc	FA5500A	1.8	2.5	3.2	V
		FA5501A	3.3	4	4.7	V

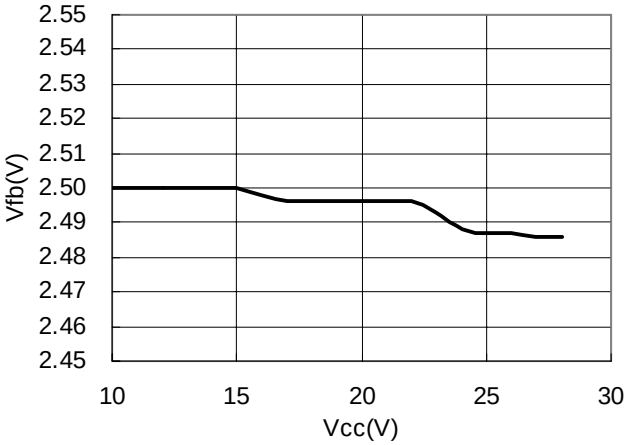
TOTAL DEVICE (VCC Pin)

Item	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Zener Voltage	Vz	Icc=25mA	30	33	36	V
Startup Power Supply Current	Istart	Vcc=8.0V	-	-	20	µA
Operating Power Supply Current	Icc	Vcc=12V		1.0	2.0	mA
Dynamic Operating Power Supply Current	Iop	50kHz,CL=1.0nF		2.0	4.0	mA

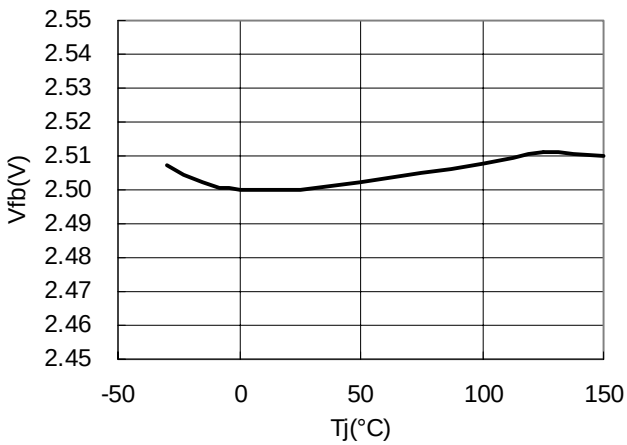
8. Characteristics curves

(Unless otherwise specified, Ta=25°C and Vcc=12V)

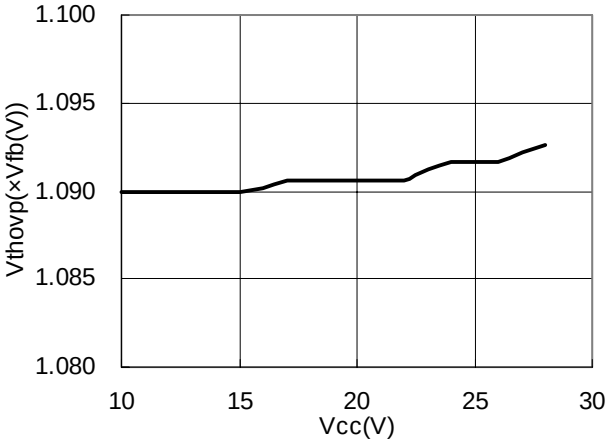
Error amplifier voltage feedback input threshold(Vfb) vs. supply voltage(Vcc)



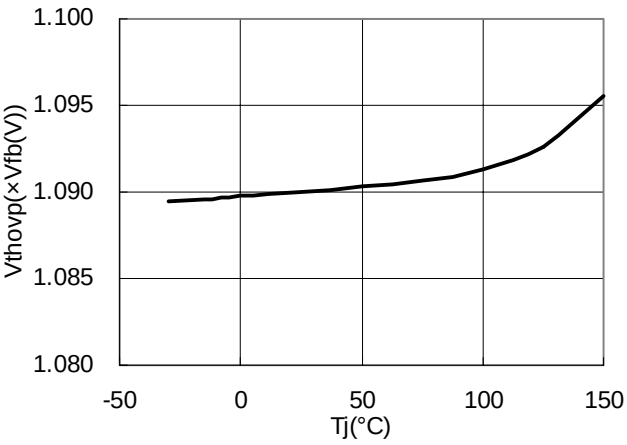
Error amplifier voltage feedback input threshold(Vfb) vs. junction temperature(Tj)



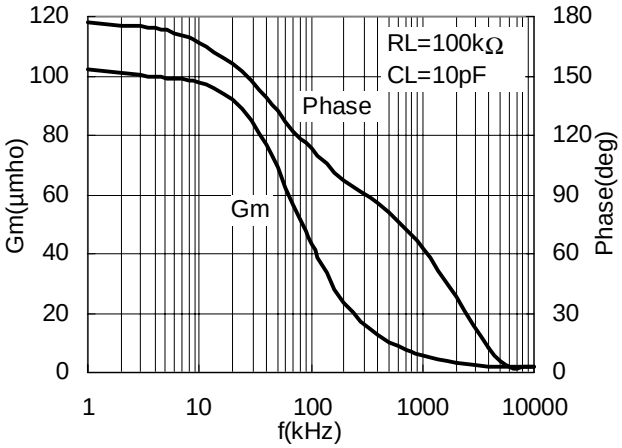
Overvoltage comparator input threshold (Vthovp) vs. supply voltage(Vcc)



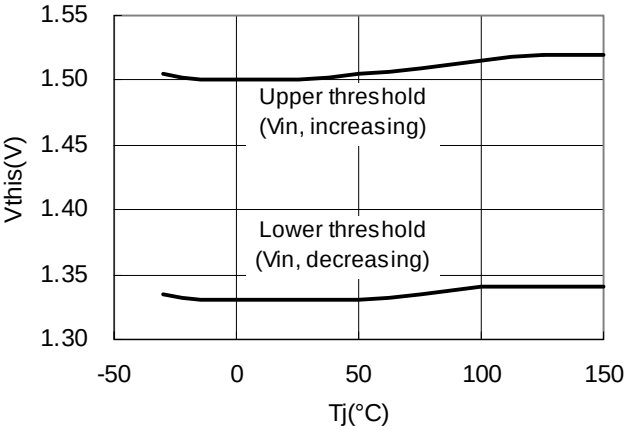
Overvoltage comparator input threshold (Vthovp) vs. junction temperature (Tj)



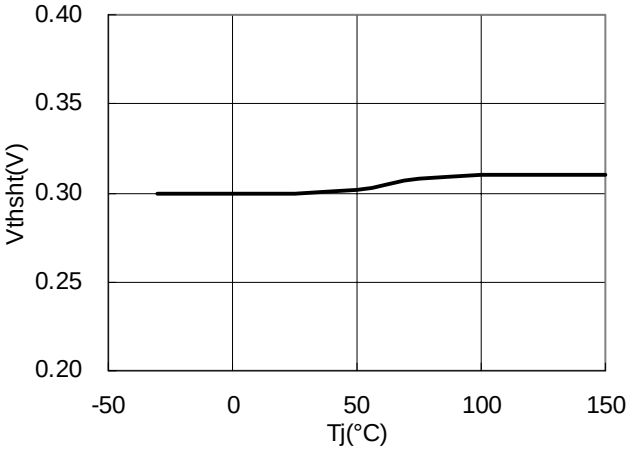
Error amplifier transconductance(Gm) and phase vs. frequency(f)



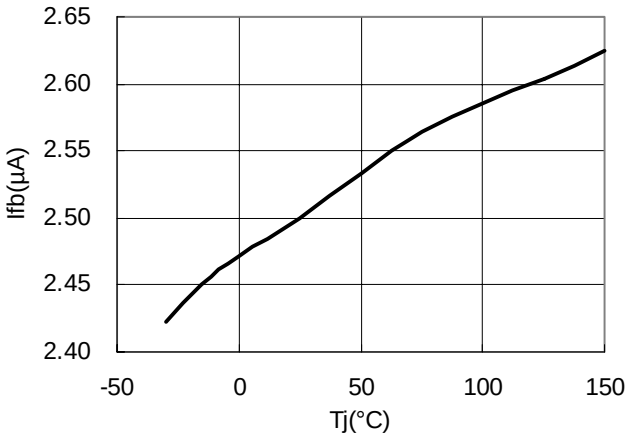
ZCD input hreshold voltage(Vthzcd) vs. junction temperature(Tj)



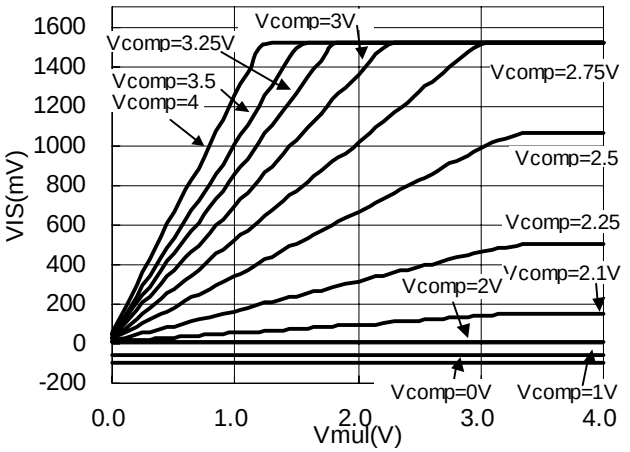
FB short compraor input threshold(Vthsht) vs. junction temperature(Tj)



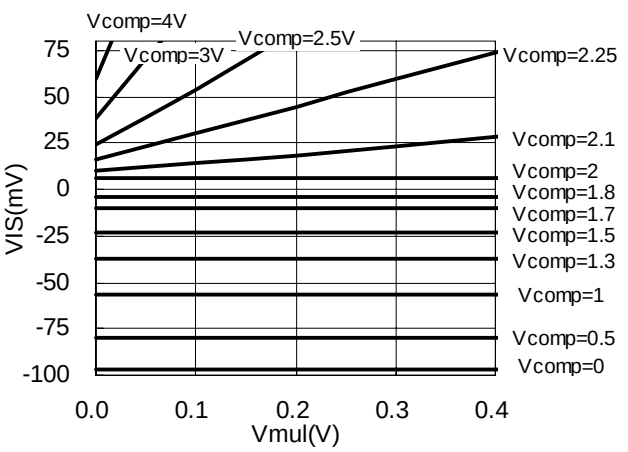
FB short comparator pulldown current(Ifb) vs. junction temperature(Tj)



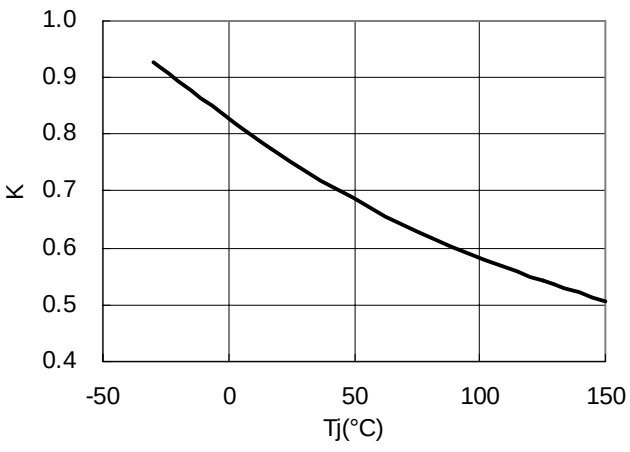
Current sense comparator thershold(VIS) vs. MUL input voltage(Vmul)



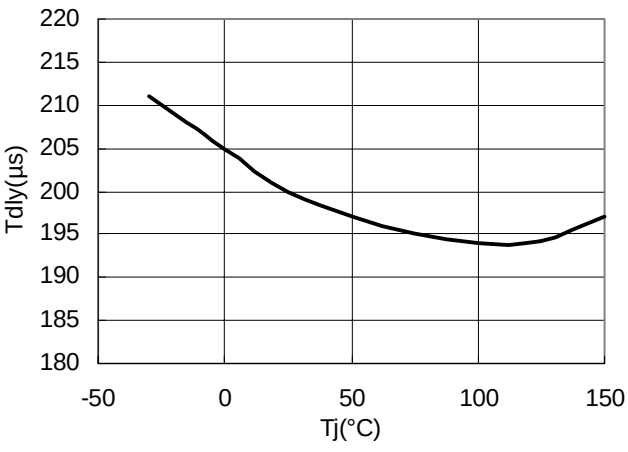
Current sense comparator thershold(VIS) vs. MUL input voltage(Vmul) (enlarged)



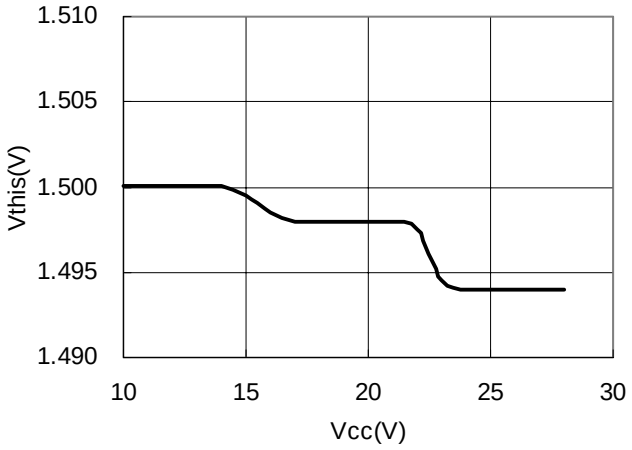
Multiplier gain(K) vs. junction temperature(Tj)



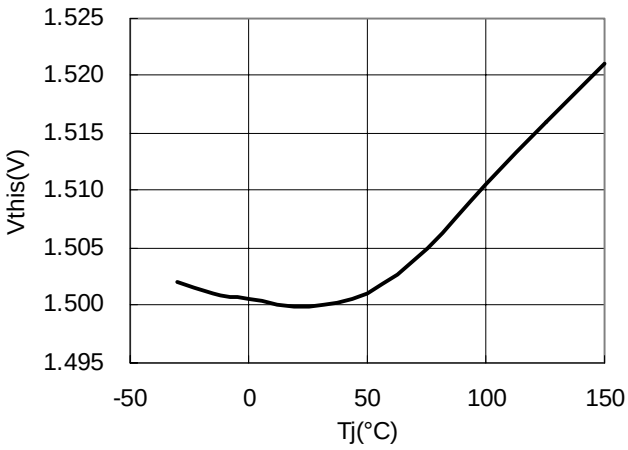
Restart timer deley time(Tdly) vs. junction temperature(Tj)



Current sense comparator maximum threshold(Vthis) vs. supply voltage(Vcc)

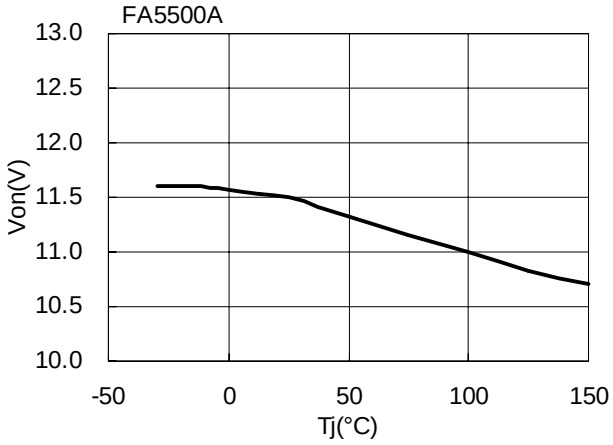


Current sense comparator maximum threshold(Vthis) vs. junction temperature(Tj)



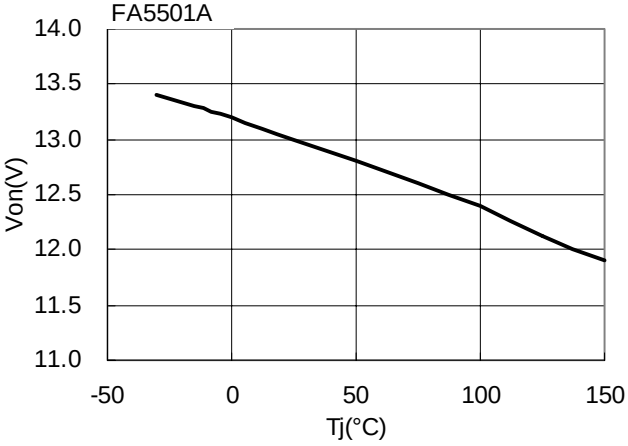
UVLO startup threshold(Von) vs. junction temperature(Tj)

FA5500A

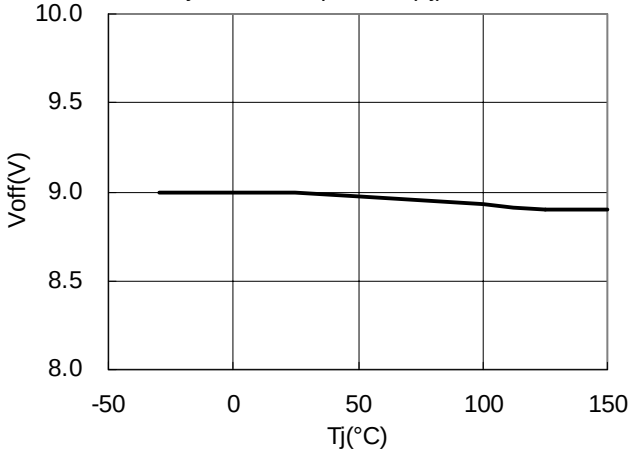


UVLO startup threshold(Von) vs. junction temperature(Tj)

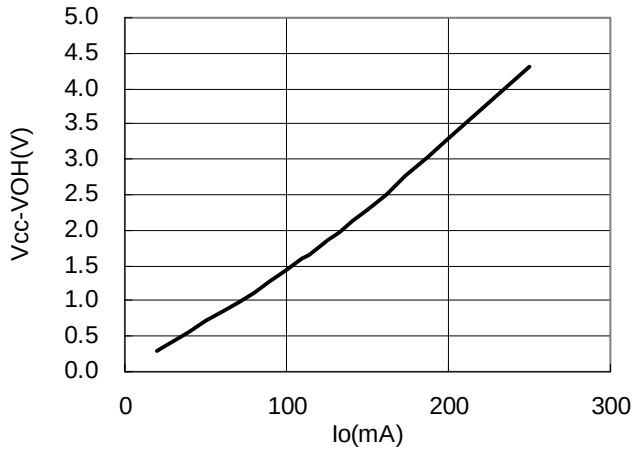
FA5501A



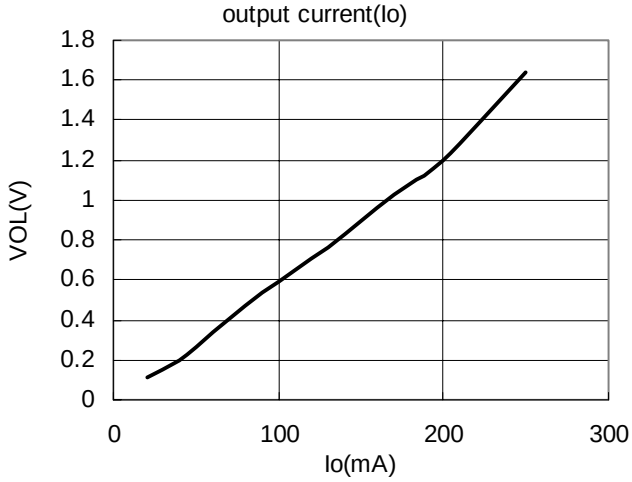
UVLO minimum operating voltage(Voff) vs. junction temperature(Tj)



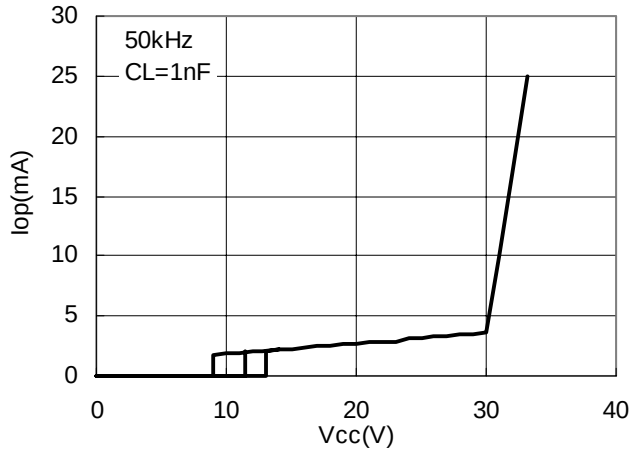
OUT pin high state voltage(VOH) vs. output current(Io)



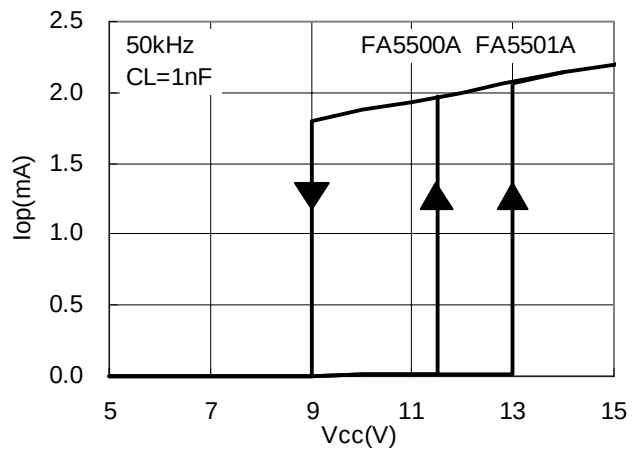
OUTpin low state voltage(VOL) vs. output current(Io)



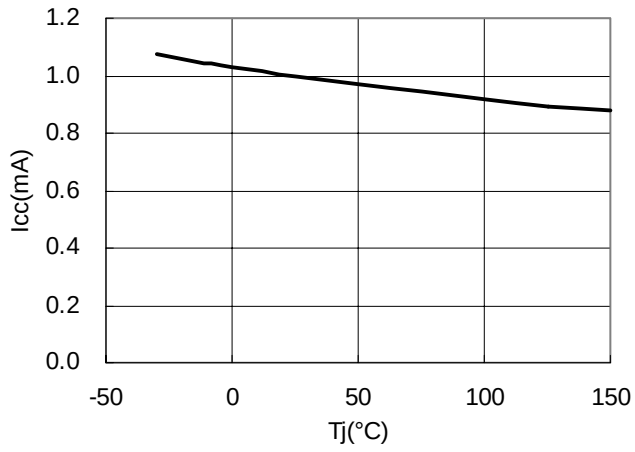
Dynamic operating power supply current(Iop) vs. supply voltage(Vcc)



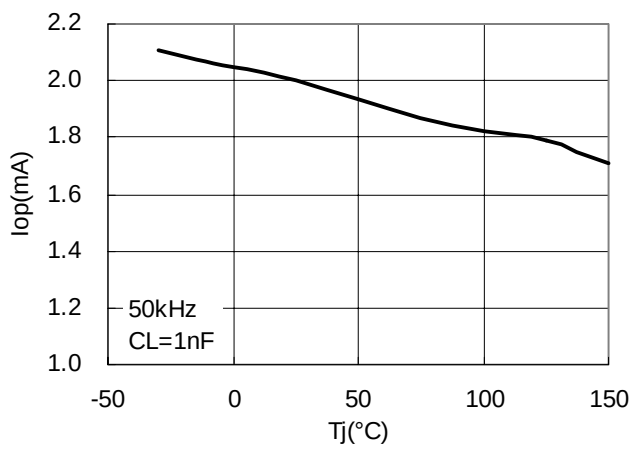
Dynamic operating power supply current(Iop) vs. supply voltage(Vcc) (enlarged)



Operating power supply current(Icc) vs. junction temperature(Tj)



Dynamic operating power supply current(Iop) vs. junction temperature(Tj)



9. Description of PFC converter

FA5500A/FA5501A are control ICs for a power factor correction converter using a boost type topology that operates in critical conduction mode. The operations, which are (1) Switching operation and (2) Power factor correction operation, are described here with the circuit shown in Fig. 1.

(1) Switching operation

This IC operates in critical conduction current mode and does not use a fixed frequency oscillator for switching operation. The waveform of each part in switching operation in steady state is shown in Fig. 2. The operation is described in detail below:

t1. When Q1 turns on, the inductor current (I_{L1}) rises from zero.

t2. When the inductor current reaches up to the threshold of the current comparator (CUR.comp.) set by the multiplier (MUL), CUR.comp. resets R-S flip-flop and then Q1 turns off. When Q1 is off, the voltage of L1 reverses polarity and the L1 current (I_{L1}) decreases supplying a current through D1 to the output. During this period, the voltage of the auxiliary winding (Vsub) also reverses polarity, then the positive voltage occurs.

t3. When I_{L1} reaches zero, the voltage of L1 drops rapidly. At the same time, Vsub also drops rapidly.

t4. When Vsub drops below 1.33V (the threshold of ZCD. comp.), the output of zero current detector (ZCD. comp.) turns to low and sets R-S flip-flop. Then Q1 turns on, and the next switching cycle starts. (Back to t1)

By repeating the steps from t1 to t4, the switching operation continues in critical conduction mode.

In the PFC converter that operates in critical conduction mode, the switching frequency always changes according to the instantaneous AC line voltage. In addition, the switching frequency also changes when the AC line voltage or the load changes.

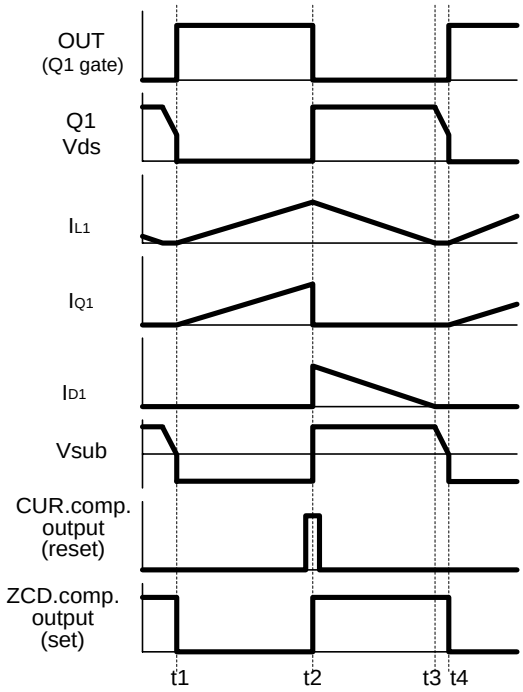


Fig.2 Timing chart of switching operation

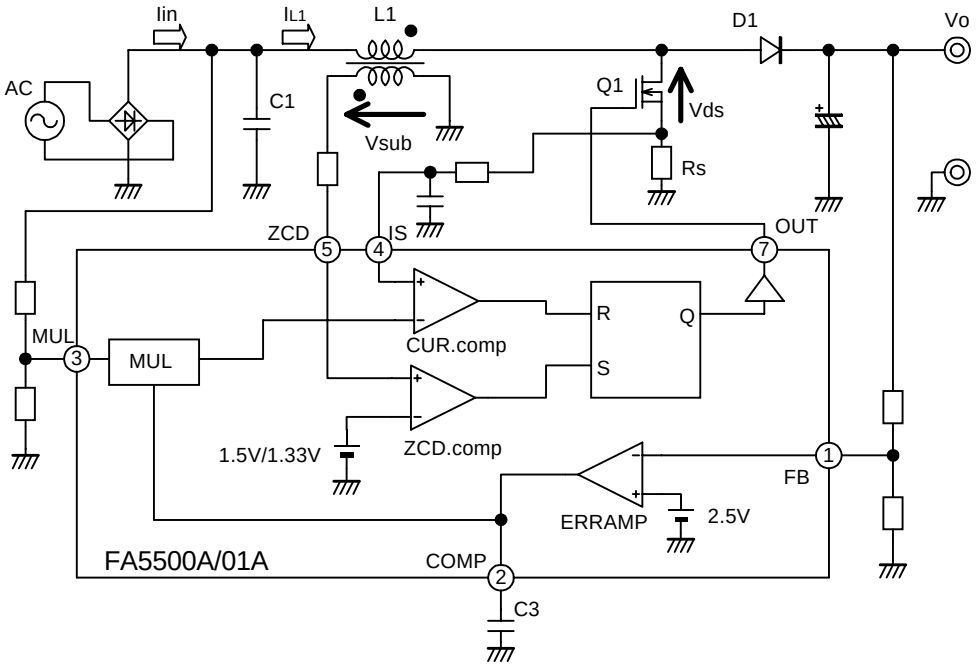


Fig.1 Outline of PFC converter circuit

(2)Power factor correction operation

As described in “(1) Switching operation”, inductor current is repeated triangular waveform. The average current ($I_{L1(mean)}$) of this repeated triangular waveform is one half of the peak current ($I_{L1(peak)}$).
Then, the inductor peak current is controlled to be sinusoidal and the high frequency content of inductor current is filtered. As a result, it is possible to force the AC input current into sinusoidal waveform.

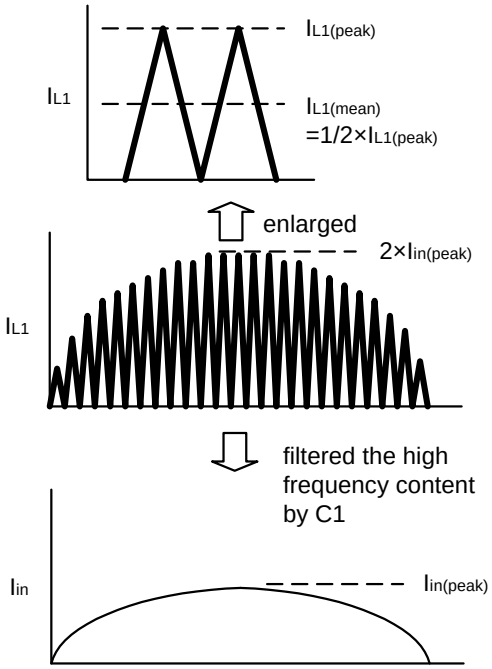


Fig.3 Outline of inductor and AC input current

In an actual circuit, the internal multiplier (MUL) controls the inductor peak current as sinusoidal waveform.

The voltage of COMP pin, which is the output of error amplifier (ERRAMP), is almost DC voltage in steady state by C3. This voltage is input to the multiplier. The other input of multiplier monitors the rectified waveform of AC line voltage. As a result, the multiplier outputs the sinusoidal waveform that is proportional to AC line voltage as the product of two input voltages.
This sinusoidal voltage is input to the current comparator (CUR. comp.) as the threshold of inductor current.

As a result, the inductor current becomes repeated triangular waveform of which peak current envelope is sinusoidal. The switching ripple of inductor current is then filtered by C1 and AC input current becomes sinusoidal waveform.

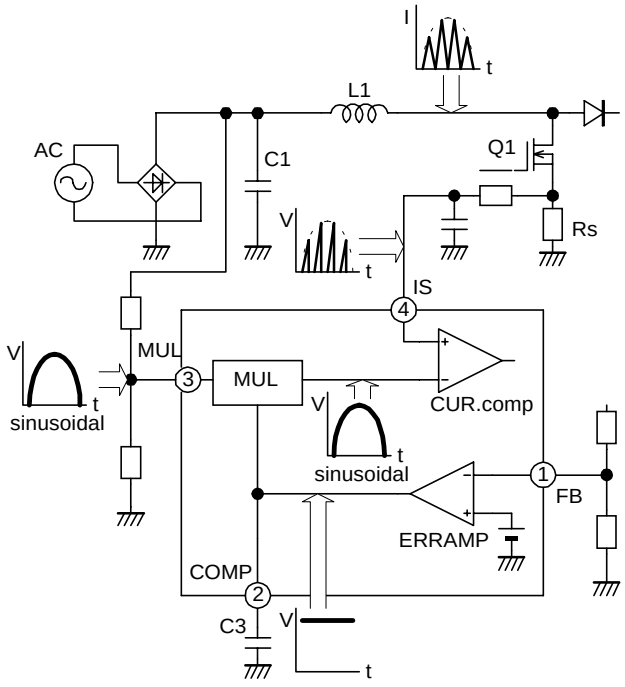


Fig.4 Outline of waveform of each part

10. Description of each circuit

(1)Error amplifier

The error amplifier controls the output voltage of PFC converter to be constant. The amplifier is a transconductance type, which has controlled voltage-to-current gain.

The non-inverting input is internally connected to the reference voltage of 2.5 V (typ.) and the inverting input is pinned out to FB pin. The output of PFC converter is divided down by resistor and monitored by the FB pin. In addition, 2.5µA of constant-current source is internally connected to the FB pin for “Open/short protection at FB pin”.

The output of error amplifier is connected to the multiplier. According to the dynamic range of multiplier, the output voltage of error amplifier ranges from 2.04 V to 3.54 V (typ.) in normal operation. The lower output voltage of error amplifier is limited by a diode connected between the input and the output of error amplifier, in order to prevent over drop in a transient condition such as rapid change of the load.

The output voltage of PFC converter contains low frequency ripple voltage associated with 2X the line frequency. If too much ripples appear at error amplifier. output, the PFC converter does not operate stable. Therefore, a capacitor is connected between COMP pin (the error amplifier output) and GND so that the cutoff frequency is set to about 20Hz in order to suppress the ripple voltage.

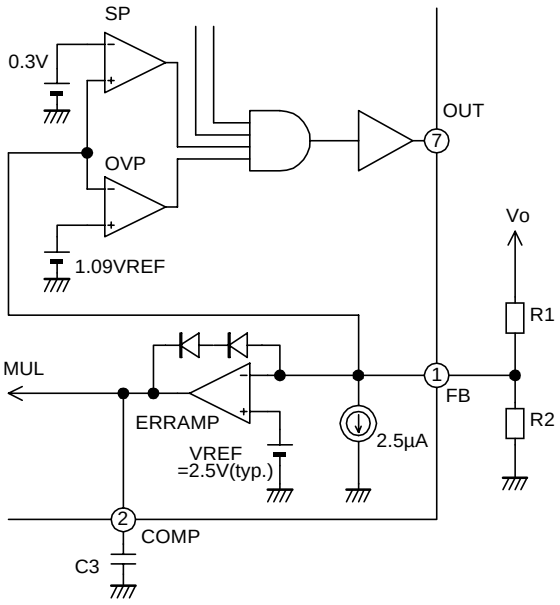


Fig.5 Error amplifier circuit

(2)Overvoltage limiting circuit

This circuit prevents the PFC output voltage exceeding the programmed voltage. The output voltage may exceed the voltage programmed by error amplifier when the converter starts up or the load changes rappidly. This circuit limits rise of the output voltage in such cases.

As shown in Fig. 5, the overvoltage limiting circuit consists of a comparator (OVP) with threshold voltage, which is set to 1.09 times of the reference voltage (VREF).

In normal operation the FB pin voltage is approximately 2.5 V, roughly the same as the reference voltage VREF. If the PFC output voltage rises more than normal voltage and then the FB pin voltage reaches the threshold of OVP comparator, the output of the comparator (OVP) turns to low and stops output pulses.

When the output voltage comes back to normal, output pulses appear again.

(3)Open/short protection at FB pin circuit

In the circuit shown in Fig. 6, if FB pin cannot monitor the PFC output voltage because of a short-circuit failure in voltage dividing resistor R2 or an open failure in R1, the PFC output voltage abnormally rises. The overvoltage limiting circuit does not operate either in this case, because the output voltage is not monitored.

To avoid these, this IC features a open/short protection at FB pin circuit. This circuit consists of a comparator (SP) with threshold voltage of 0.3V (typ.). If the input voltage of FB pin drops below 0.3V due to a short-circuit failure in R2 or an open failure in R1, the output of comparator (SP) turns to low and stops the output pulses.

In the PFC converter, because of a boost type topology, the voltage rectified the AC line is supplied to the PFC output even before the converter operates. Therefore, if the PFC converter is normal, voltage is always applied to FB pin and this protection circuit does not operate.

If an open failure occurs between FB pin and the voltage divider, the FB pin voltage is forced to lower by the 2.5µA of constant current source internally connected to FB pin. Then comparator (SP) stops the output pulses in the same way.

If the FB pin voltage comes back to normal after this protection circuit operates, output pulses appear again.

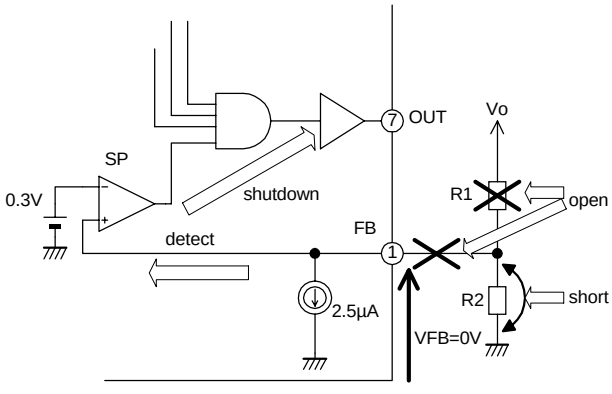


Fig.6 Open/short protection at FB pin

(4)Multiplier

The multiplier is a circuit to control input current into sinusoidal waveform.

One of the inputs is connected to MUL pin. The rectified AC line voltage is divided down by resistor and monitored by MUL pin. The other input is internally connected to the output of error amplifier. Typically, the output of error amplifier is almost DC over a given AC line cycle. Therefore, the multiplier outputs the sinusoidal voltage of which amplitude changes in proportion to the output of error amplifier. This output becomes the threshold of current comparator and the AC input current is controlled into sinusoidal waveform.

Based on the dynamic range of multiplier, the peak voltage applied to MUL pin should be within 2.5 V in normal operation.

The rectified AC line voltage contains much switching noises from Q1. To avoid the influence of the noises, a capacitor (C6) is connected for a filter.

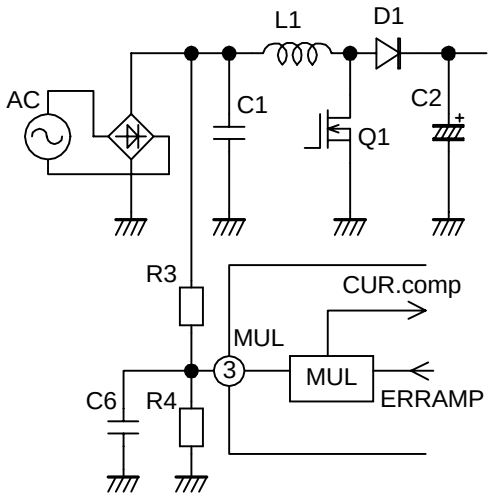


Fig.7 Multiplier circuit

(5)Current sense comparator

One of the inputs is internally connected to the output of multiplier as the threshold. The other input is connected to IS pin to monitor the MOSFET source current converted to voltage by current sense resistor (Rs). In each switching cycle, when MOSFET current reaches up to the threshold determined by the multiplier, the output of current comparator turns high and reset the RS flip-flop. As a result, MOSFET turns off, and the on cycle of MOSFET is over.

The threshold voltage of current comparator is internally clamped to 1.8V (max.). Therefore, when PFC starts up or load and input voltage changes rapidly, the maximum current of MOSFET is limited at the value calculated with the following equation:

$$Id(max.) = \frac{1.8}{Rs}$$

To prevent malfunction by noises, RC filter is typically connected between IS pin and the current sense resistor Rs.

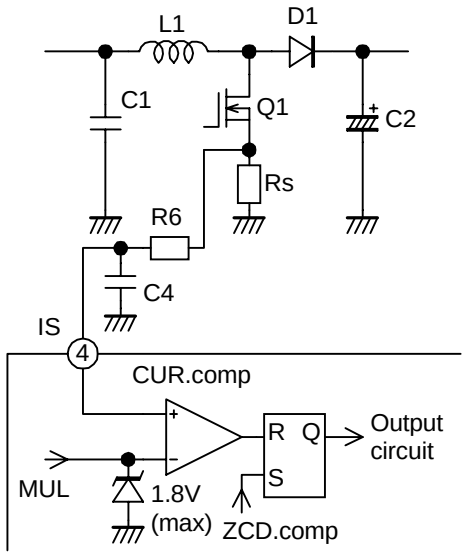


Fig.8 Current sense comparator circuit

(6)Zero current detector

This IC operates in critical conduction current mode without a fixed frequency oscillator. The zero current detector circuit (ZCD) detects the inductor current reaches zero to turn the MOSFET on at the next switching cycle.

The voltage of auxiliary winding (sub) is monitored by ZCD pin as shown in Fig. 9. During OFF period of MOSFET, positive voltage occurs in the auxiliary winding. When the inductor current reaches zero, the voltage of auxiliary winding falls rapidly. ZCD.comp. detects it and sets the RS flip-flop to turn the MOSFET on at the next switching cycle.

The voltage of auxiliary winding varies significantly according to input and output voltage. To protect the IC against the various voltages, a clamp circuit is built in with the upper limit of 7.6V(typ.) and the lower limit of 0.6V(typ.).

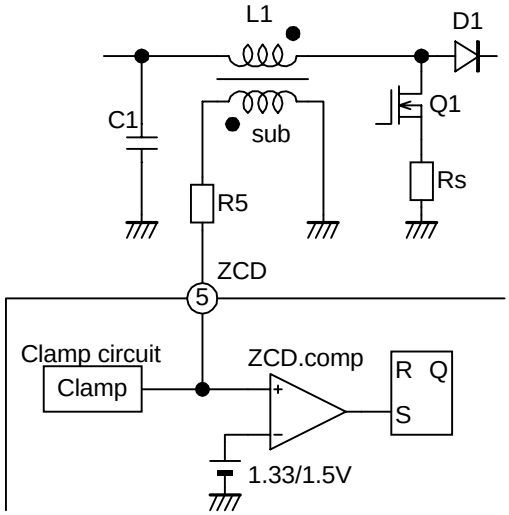


Fig.9 ZCD circuit

A resistor for current limit is typically connected between the ZCD pin and the auxiliary winding because of rating current of ZCD pin.

A current out of or into the ZCD pin should be within 3mA so that the IC will operate normally.
On the other hand, if the current out of or into the ZCD pin is too small, unstable operation may occur. Therefore, current limiting resistor of R5 should be below 47kΩ.

While MOSFET is on, negative voltage is generated in the auxiliary winding. A current flows out of the clamp circuit and the ZCD pin voltage is clamped to 0.6V (typ.). While MOSFET is off, positive voltage is generated in the auxiliary winding. A current flows into the clamp circuit and the ZCD pin voltage is clamped to 7.6V (typ.).

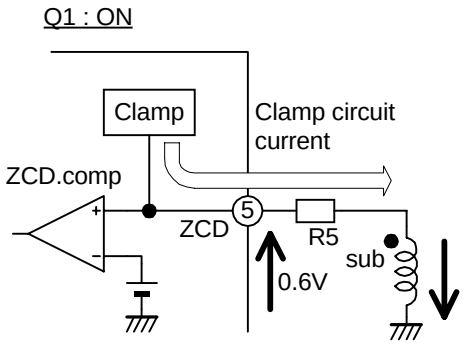


Fig.10 Clamp circuit of ZCD pin(1)

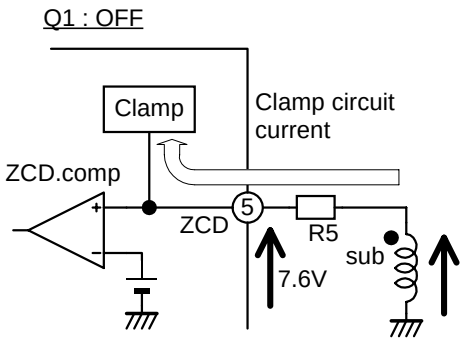


Fig.11 Clamp circuit of ZCD pin(2)

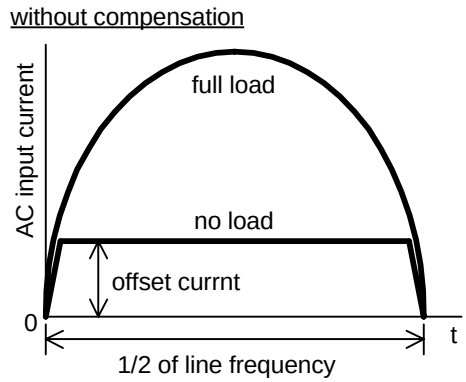
(7)Compensation circuit for light load

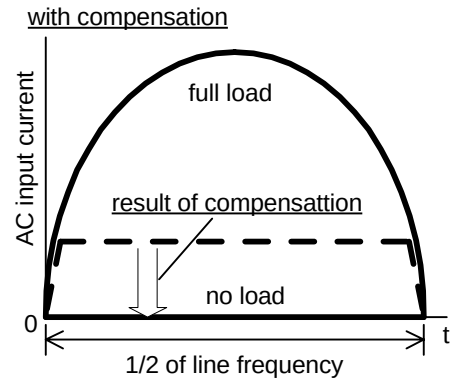
If the output of multiplier, which determines the threshold of current comparator, does not have offset voltage, the input current to the converter is approximately zero under condition that the PFC converter operates in no load. But an actual multiplier may have offset voltage. If the offset voltage is positive, the input current, which corresponds to the offset voltage, flows into the converter even when the PFC converter operates in no load. In this case, the PFC output voltage rises abnormally because of too much input current.

To avoid these, this IC has an automatic offset correction circuit (AOC) for light load. The output voltage of error amplifier is approximately 2V or higher in normal operation. When the output voltage of error amplifier drops below 2V, AOC circuit operates.

If the output of multiplier has a positive offset, the output voltage of error amplifier falls below 2V in the case that the PFC converter operates in no load or light load. Then, the offset voltage is corrected in the current comparator by AOC circuit. Because of this operation, even in the no load or light load condition, the PFC output voltage does not rise abnormally, but is always kept constant. The amount of correction changes linearly according to the output of error amplifier so that the operation can be made stable.

Input current





Output voltage

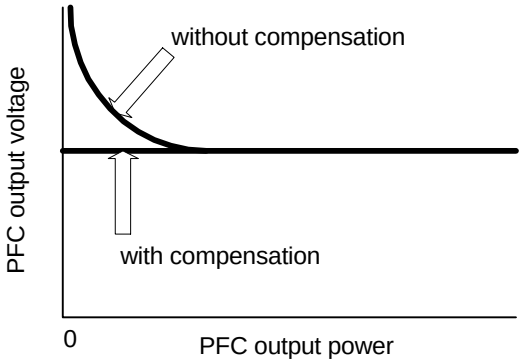


Fig.12 Outline of operation when multiplier has a positive offset

(8)Restart timer

In steady state, set signals from the ZCD circuit turns MOSFET on at each switching cycles. But a trigger signal is needed when starting up or stabilizing operation in the light load condition. This IC includes a restart timer. If off period of output pulse continues 200µs or more, it automatically generates a trigger signal.

(9)Undervoltage lockout circuit

These IC contain an undervoltage lockout circuit to prevent malfunction when the supply voltage drops. When the supply voltage rises from 0V, FA5500A starts operation at 11.5V(typ.) and FA5501A starts operation at 13V(typ.). If the supply voltage drops after the IC starts up, both IC stops operation at 9V(typ.). When IC stops operation by undervoltage lock out circuit, OUT pin voltage is kept in low state and the current consumption of IC decreases below 20µA.

(10)Output circuit

This IC contains a push-pull output stage and can directly drive the MOSFET. The peak current of output stage is sink: 1.0A (max.), source: 0.5A (max.)

11. Design advice

(1)Designing a PFC converter

The following description is a sample of designing of a PFC converter with FA5500A/FA5501A using a circuit shown in Fig. 13. However, this is just a sample of calculating. If you want to use the components or circuits calculated in this process, be sure to test and determine in actual circuit. In addition, be sure to consider and check the characteristics, the tolerance and the rating of each component including this IC.

(1-1) Specification of PFC converter

To begin designing, the following specification of PFC converter is determined.

Input voltage range (Vrms): Vac(min.) to Vac(max.)
Output voltage (V): Vo (> $\sqrt{2}$ ×Vac (max.))
Maximum Output power(W): Po

Output voltage (Vo) should be set higher than the peak value of input voltage (= $\sqrt{2}$ ×Vac (max.)) because the PFC converter is a boost type topology.

(1-2) Designing inductance of L1

The switching frequencies are determined with input-output conditions and the value of inductor because PFC converter operates in critical conduction mode (see Supplement). Therefore, the value of inductor L1 (Lp) can be determined with input-output conditions and the minimum operating frequency.

When efficiency of PFC is η and the minimum operating frequency is fsw (min.), Lp is calculated by following equation.

$$Lp=\frac{Vac_{(min.)}{}^2\times(Vo-\sqrt{2}\times Vac_{(min.)})\times\eta}{2\times fsw_{(min.)}\times Po\times Vo}$$

It is recommended to set fsw(min) between 20kHz-100kHz. Assume that the efficiency η is approximately 90% in calculating.

Supplement: Inductance and switching frequencies

On and off period of each switching cycle can be calculated with the following equation.

$$Ton=\frac{2\times Lp\times Po}{Vac^2\times\eta}$$

$$Toff=\frac{2\times Lp\times Po}{Vac^2\times\eta\times\left(\frac{Vo}{\sqrt{2}\times Vac\times|\sin\omega t|}-1\right)}$$

where,
ω=2×π×fac
fac: AC line frequency (Hz)

In theory, according to the equation above, if input-output conditions are constant, Ton is also constant. On the other hand, Toff changes corresponding to each instantaneous voltage of AC line, maximum at ωt =90°, minimum at ωt =0°. Then, switching frequencies can be calculated with the following equation according to the relationships described above:

$$fsw=\frac{Vac^2\times\left(Vo-\sqrt{2}\times Vac\times|\sin\omega t|\right)\times\eta}{2\times Lp\times Po\times Vo}$$

The switching frequencies always change corresponding to each instantaneous voltage of AC line.

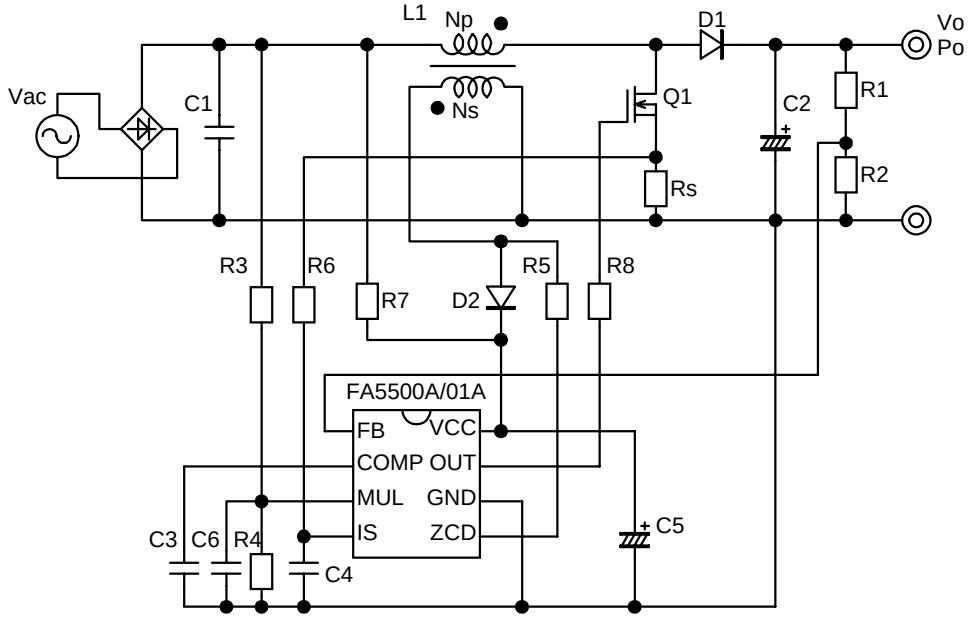


Fig.13 Typical application circuit

(1-3) Designing auxiliary winding of L1

The auxiliary winding typically has two functions:
-Detecting that inductor current reaches zero
-Supplying Vcc voltage of IC
To achieve these functions, you have to determine a proper ratio of it to the main winding.

The voltage of auxiliary winding always changes according to each instantaneous voltage of AC line. The outline of the auxiliary winding voltage is shown in Fig. 14.

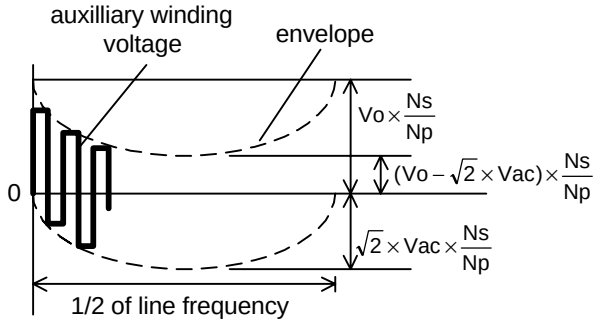


Fig.14 Auxiliary winding voltage

The following conditions should be satisfied based on this various voltage.

ZCD Threshold Voltage

The threshold voltage of ZCD comparator is 1.87V(max.) when ZCD pin voltage rises. It is necessary for the minimum voltage of auxiliary winding to exceed this threshold voltage. Therefore, the following condition must be satisfied.

$$Ns/Np > \frac{1.87}{\left(Vo - \sqrt{2} \times Vac_{(max.)}\right)}$$

Vcc voltage

The following condition must be satisfied, so that Vcc voltage will be set between 12V and 28V according to the recommended condition.

$$\frac{12}{Vo} < Ns/Np < \frac{28}{Vo}$$

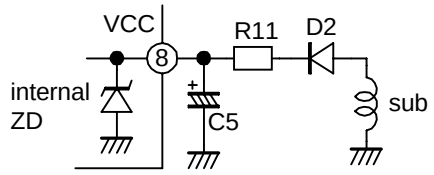
The turns ratio Ns/Np must satisfy both two condition.

If the boost voltage ratio of PFC (the ratio of Vo to Vac) is too small, the turns ratio can not satisfy both condition. This problem can be solved with following methods.

-Attach two auxiliary windings for both ZCD and Vcc respectively.

-Set ZCD condition preceding Vcc condition. In this case, there is possibility for Vcc to exceed the recommended conditions. Therefore, clamp the Vcc with internal ZD or additional ZD (Fig. 15). In this case, a resistance for current limit (R11) is needed between the auxiliary winding and Vcc pin. In addition, especially when using internal ZD, mind that "Total power supply and zener current" and "Power dissipation" must not exceed the absolute maximum rating value.

using internal ZD



using external ZD

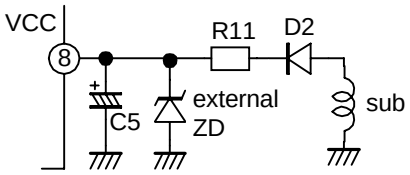


Fig.15 Vcc clamp circuit

(1-4) ZCD pin circuit

The auxiliary winding voltage is monitored by ZCD pin in order to detect that the inductor current reaches zero. A resistor for current limit (R5) is connected between ZCD pin and the auxiliary winding because of rating current of ZCD pin. The most appropriate value of R5 is determined by evaluating in the actual circuit.

However, a current out of or into the ZCD pin should be within 3mA as shown in the recommended operating conditions so that the IC will operate normally. Therefore, the following conditions should be satisfied.

For lower clamp

$$R5 > \frac{1.0 + \sqrt{2} \times Vac(max.) \times \frac{Ns}{Np}}{3 \times 10^{-3}}$$

For upper clamp

$$R5 > \frac{Vo \times \frac{Ns}{Np} - 7.0}{3 \times 10^{-3}}$$

On the other hand, if the current out of or into the ZCD pin is too small, unstable operation may occur. Therefore, current limiting resistor of R5 should be below 47kΩ.

$R5 < 47k\Omega$

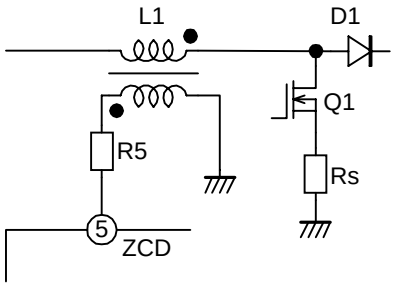


Fig.16 ZCD pin circuit

In actual circuit, the value of R5 also influences MOSFET switching.

MOSFET(Q1) turns on when the current of inductor L1 reaches zero. Just before turning on, the drain voltage of MOSFET (Vds) begins sinusoidal oscillation because of resonance of L1 and the parasitic capacitor. If the value of R5 is set properly, MOSFET can be turned on at the bottom of the voltage oscillation. This can minimize the switching loss and surge current at turn on. If the value of R5 is too small, MOSFET turns on too early and if it is too large MOSFET turns on too late. The adequate value of R5 depends on each circuits or input and output conditions. Therefore, determine the most appropriate value by evaluating the operation in the actual circuit.

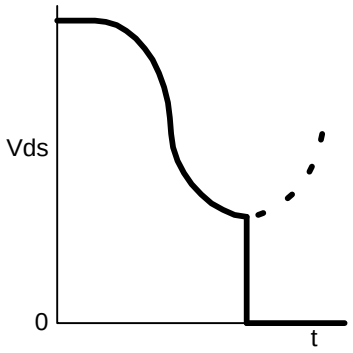
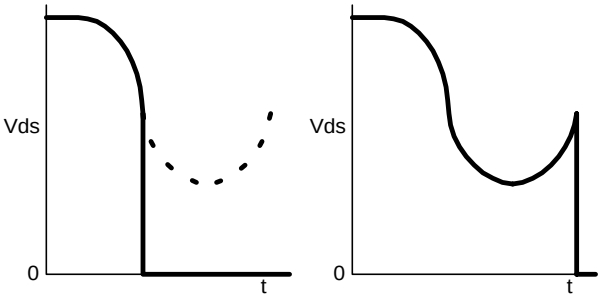


Fig.17 Vds waveform at turn on (with adequate R5)



R5 is too small. R5 is too large.

Fig.18 Vds waveform at turn on (with inadequate R5)

(1-5) Vcc Pin circuit

The startup resistor R7 should satisfy the following formula in order to supply with at least 20μA of IC startup current.

$$R7 < \frac{\sqrt{2} \times Vac(min.) - Von(max.)}{20 \times 10^{-6}}$$

Where,

Von(max.): maximum voltage of startup threshold of UVLO
FA5500A: Von(max.)=13V
FA5501A: Von(max.)=14.5V

This formula is, however, just the minimum condition to start the IC. The startup time required for PFC converter must also be decided on. The value of R7 should be tested and determined in actual circuit for appropriate startup time.

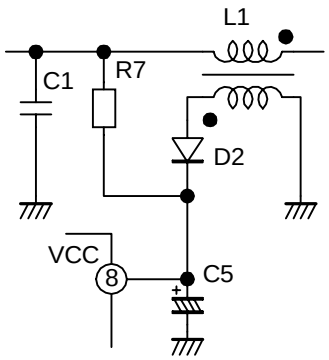


Fig.19 Vcc pin circuit

In steady state, Vcc is supplied from the auxiliary winding of inductor. When the IC is just starting up, however, it takes time for the voltage from auxiliary winding to rise enough. The value of capacitor C5 connected to Vcc pin should be determined to prevent Vcc from falling below the UVLO threshold voltage during the this period. The capacity of C5 should be tested and determined in the actual circuit because the time lag is different in each circuit.

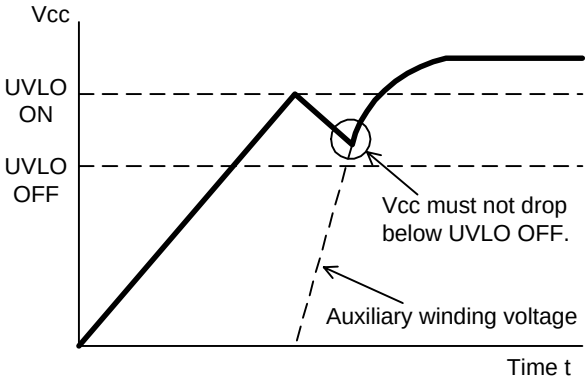


Fig.20 Vcc voltage at startup

Even after PFC starts up, Vcc may fall due to rapidly changes of the load or inputs. To prevent the IC from stopping in those cases, the circuit shown in Fig.21 is effective to prolong the hold time of the Vcc voltage. After the PFC converter starts up, Vcc is supplied through C7. Therefore, you can prolong the hold time of Vcc by using a large capacity for C7.

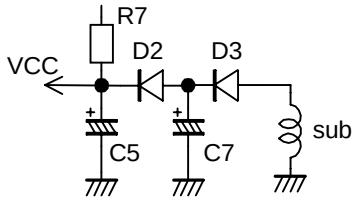


Fig.21 Vcc pin circuit (2)

In some case, the Vcc voltage cannot be supplied enough in light load condition. In this case, the circuit shown in Fig.22 may be effective to improve the Vcc. In this circuit, R10 suppress the surge current of MOSFET at turn on to prevent the malfunctions. (See (1-7) IS pin

circuit) The appropriate value of C8 and R10 should be tested and determined in actual circuit because they depend on each circuit.

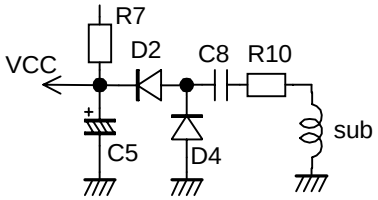


Fig.22 Vcc pin circuit (3)

(1-6) MUL Pin circuit

The input voltage of MUL pin is related to IS pin threshold voltage range. To prevent the distortion of AC input current, the value of resistor divider R3 and R4 should be determined so that the maximum peak voltage of MUL pin ($V_{MUL-P(max)}$) is below 2.5V when the AC line voltage is maximum.

$$V_{MUL-P(max)} = \sqrt{2} \times Vac(max) \times \frac{R4}{R3+R4} < 2.5[V]$$

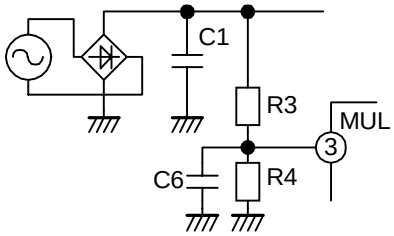


Fig.23 MUL pin circuit

In an actual circuit, the rectified voltage contains many noises from switching. To avoid this influence, a capacitor C6 is typically connected between MUL pin and GND pin. If the capacity of C6 is too small, the filtering is not effective. If the capacity is too large, the input voltage of MUL pin is distorted and then AC input current is also distorted. In calculating, the cutoff frequencies determined with C6 and R3, R4 should be set to about 1 or 2kHz.

$$\frac{1}{2\times\pi\times C6\times(R3//R4)} \approx 1 \text{ or } 2[kHz]$$

Where;

R3//R4 represents the resistance of parallel connection of R3 and R4.

(1-7) IS Pin circuit

The input current becomes the greatest when AC line voltage is minimum (Vac(min.)). Even in this case, it is necessary to set the current detector resistance Rs so that required input current can be supplied.

After setting a voltage divider connected to MUL pin, the threshold voltage range of IS pin is calculated as follows.

When AC line voltage is minimum, the minimum clamp voltage of IS pin threshold voltage ($V_{thIS-P(min)}$) can be calculated according to the characteristics of multiplier and the input voltage range.

$$V_{thIS-p(min)} = K_{(min)} \times \left(V_{MUL-P(min)} \times \left(\left(V_{thcomp}+1\right) - V_{thcomp}\right)\right) = 0.53 \times V_{MUL-P(min)} \times 1$$

Where,

$V_{MUL-P(min)}$: MUL pin peak voltage at minimum AC line voltage

$K_{(min.)}$: multiplier gain

Note:

When $V_{thIS-P(min)}$ >1.3V, use $V_{thIS-P(min)}$ =1.3V.

Set the current sense resistance Rs in order to flow necessary current even when clamp voltage is $V_{thIS-P(min)}$. The maximum of the inductor peak current ($I_{LP(max.)}$) is approximately expressed with the following equation.

$$I_{LP}(max.) = \frac{2\times\sqrt{2}\times Po}{\eta\times Vac(min.)}$$

Therefore, the value of Rs can be calculated with the following equation.

$$Rs = \frac{V_{thIS-p(min)}}{I_{LP}(max.)}$$

When MOSFET turns on, surge current caused by driving MOSFET or discharging of parasitic capacitor flows to Rs. This IC controls the peak current of MOSFET. Therefore if this surge current is too large, the AC input current can be distorted by malfunctions. In addition, depending on the magnitude or timing of surge current, irregular narrow pulses may appear on the output pulses when OUT pin goes high. Therefore, a RC filter R6 and C4 is typically connected. In order not to influence normal operation, it is necessary to set the cutoff frequency of RC filter higher than the switching frequency. In this calculation, the cutoff frequency is assumed about 1 or 2 MHz.

$$\frac{1}{2\times\pi\times C4\times R6} \approx 1 \text{ or } 2[MHz]$$

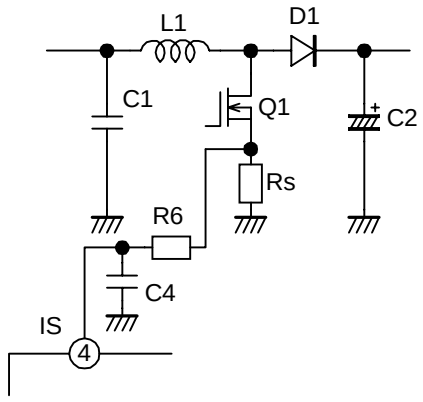


Fig.24 IS pin circuit

If the effect of RC filter is not enough, connect OUT pin and MOSFET as shown in Fig. 25 in order to reduce driving current to turn the MOSFET on. In this circuit, drive currents to turn the MOSFET on and off can be set independently.

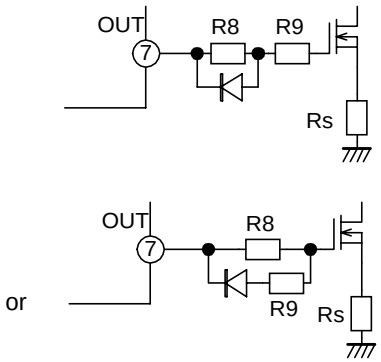


Fig.25 Gate drive circuit

The inductor current reaches zero just before the MOSFET turns on and MOSFET current rises from around zero when MOSFET is on. Therefore, even if the driving current to turn on is set small and the switching speed becomes a little slow, the loss of MOSFET does not increase extremely.

(1-8) Input/output of error amplifier

PFC output voltage Vo is divided down and input to FB pin. Vo is controlled so that the FB pin voltage is equal to the internal reference. This IC has a current source (I_{FB}) of 2.5μA(typ.) connected FB pin internally. Therefore, the relationship between Vo and the voltage divider resistor can be expressed with the following equation.

$$Vo = \frac{R1+R2}{R2} \times \left(Vref + \frac{I_{FB}}{Gm} \right) + R1 \times I_{FB}$$

where, Gm : Transconductance of error amplifier

PFC output voltage contains ripple voltage associated with twice the line frequency. If this ripple voltage appears at the output of error amplifier, PFC does not operate stably. To avoid this, a capacitor should be inserted between COMP pin and GND so that the bandwidth is set to about 20Hz. The bandwidth can be expressed with the following equation.

$$BW = \frac{Gm}{2 \times \pi \times C3}$$

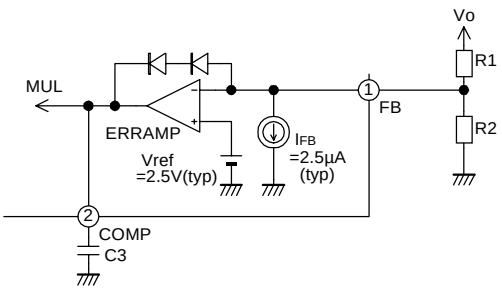


Fig.26 Input/output of error amplifier circuit

(1-9) Input/output capacitor

The input capacitor C1 rejects the switching ripples of inductor current and prevents it from flowing to AC line. Therefore, the larger C1 is, the smaller the switching ripples contained in AC input current are. But larger C1 may causes of lowering power factor.

In calculation, capacity of C1 is assumed as 1μF per 1A of maximum AC input current. The most appropriate capacity should be determined by evaluating power factor and AC line noises in the actual circuit.

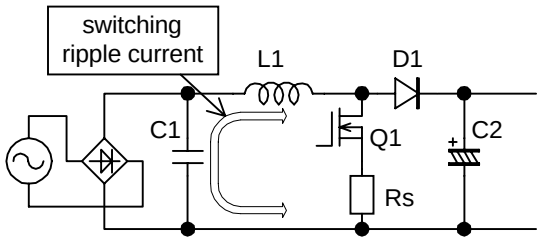


Fig.27 Input capacitor circuit

PFC output contains ripple voltage of twice the line frequency. The output capacitor C2 suppresses this ripple voltage.

The ripple voltage appearing on the output voltage can be expressed by the following equation.

$$V_{ripple(0-p)} \approx \frac{Io}{2 \times \omega \times C2}$$

where,
$\omega = 2 \times \pi \times fac$
fac: AC line frequency [Hz]

If the output voltage including ripple voltage reaches up to the overvoltage threshold, the IC cannot operate properly. Therefore, C2 should be selected satisfying the following equation.

$V_{ripple(0-p)} < 0.075 \times Vo$

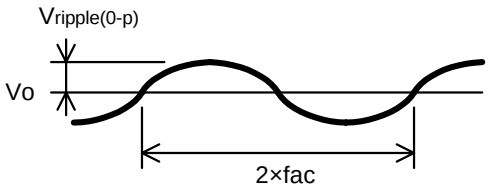


Fig.28 Output ripple voltage

(2)Improving operation around zero-crossing

The dead time of AC input current may appear around zero crossing. A high value resistor R12 (several 100k or several MegΩ) connected between MUL pin and Vcc pin may reduce the dead time. But too much correction, which means connecting too small resistance, causes distortion of AC input current or overvoltage at light load. Be careful when R12 is connected.

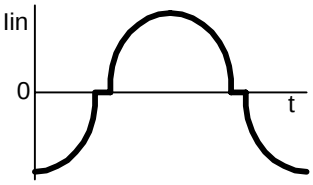


Fig.29 Input current including dead time

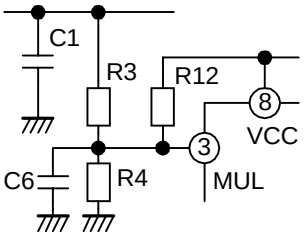


Fig.30 Compensation circuit of dead time

On the other hand, surge current may appear around zero crossing in some application.
This surge current can influence harmonic currents. In this case, a high value resistor R13 (several 100k or several MegΩ) connected between IS pin and Vcc pin may suppress this surge current.

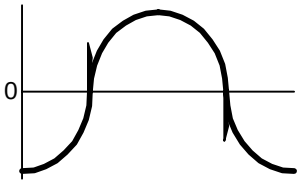


Fig.31 Input current including surge current

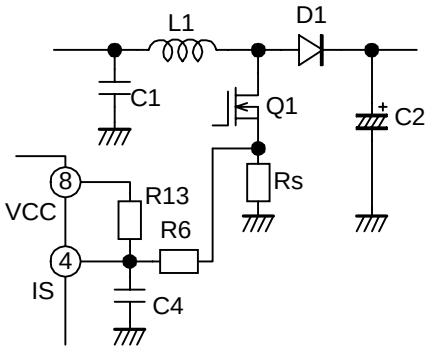


Fig.32 Compensation circuit of surge current

(3)Prevent malfunction caused by negative voltage applied to a pin

When large negative voltage is applied to each IC pin, a parasitic element in the IC may operate and cause malfunction. Be careful not to allow the voltage applied to each pin to drop below -0.3V. Especially for the OUT pin, voltage oscillation caused after the MOSFET turns off may be applied to the OUT pin via the parasitic capacitance of the MOSFET, causing the negative voltage to be applied to the OUT pin. If the voltage falls below -0.3V, add a Schottky diode between the OUT pin and the ground. The forward voltage of the Schottky diode can suppress the voltage applied to the OUT pin. Use the low forward voltage of the Schottky diode.

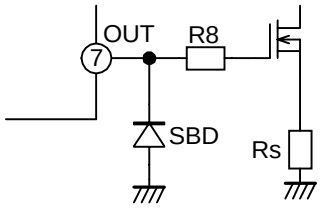


Fig.33 Protection circuit of OUT pin against the negative voltage

Similarly, be careful not to cause the voltages at other pins to fall below -0.3V.

(4)Prevent malfunction caused by noise

Noise applied to each pin may causes malfunction of IC. Capacitor of RC filter for IS pin and MUL pin should be connected as close as possible to suppress noise effectively.

Noise applied to COMP pin may also cause malfunction. The capacitor between COMP and GND pin should be connected as close as possible, too.

(5)Open/short protection at FB pin

This IC has Open/short protection at FB pin circuit, which shuts off output, if complete open circuit or short circuit failures may occur on voltage divider for monitoring PFC output voltage. But, if voltage divider resistance varies because of degradation, this circuit may not protect enough. Therefore, be sure to consider and evaluate your set, component characteristics and the like sufficiently, and then design an additional protection circuit if needed.

(6)ON/OFF operation by external signal

The following methods make it possible to turn on or off the PFC by external signal.

(i) Shut down supply voltage to Vcc pin

To shut down supply voltage to Vcc pin by external signals leads IC's shut down.

(ii) Lower COMP pin voltage below Vthcomp

It can stop the output pulses to lower COMP pin voltage below Vthcomp. In this case, lower COMP pin voltage below 1V, considering temperature characteristic and so on. An example circuit is shown in Fig. 34.

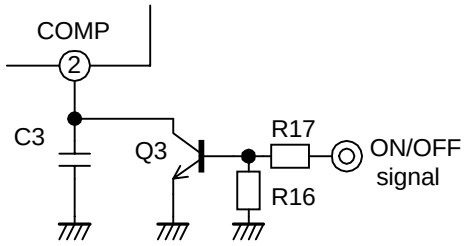


Fig.34 ON/OFF control circuit (1)

If the discharging current of capacitor C3 should be limited, connect a resistor R19 as shown in Fig. 35. The value of R19 should be selected 1kΩ or smaller. In addition, check that COMP pin voltage is lowered below 1V.

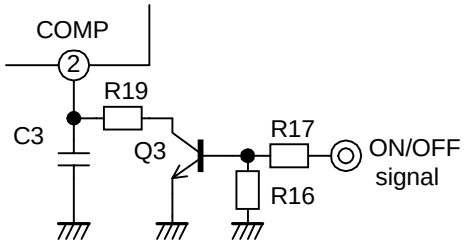
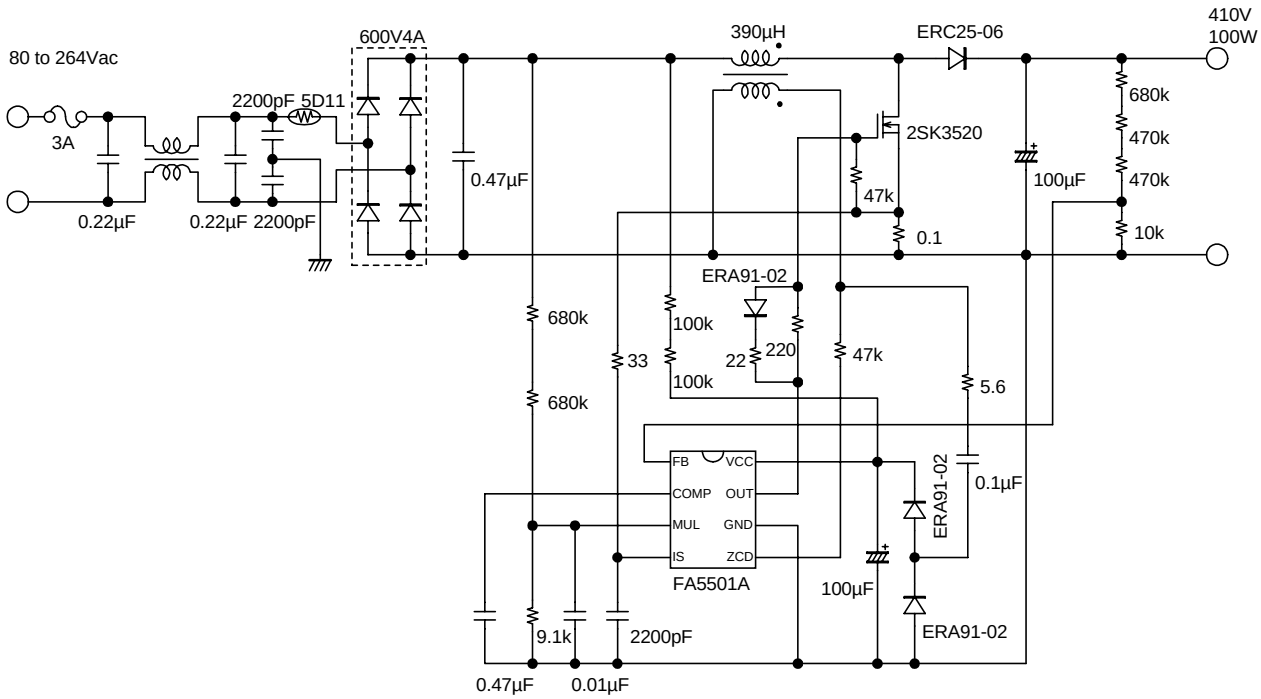


Fig.35 ON/OFF control circuit (2)

When lowering COMP pin voltage, in addition to the output current of error amplifier, current, which flows voltage divider connected FB pin, appears at COMP pin through diode connected between input and output of error amplifier. When designing and evaluating the circuit, consider this current sufficiently, too. (See 10. Description of Each Circuit (1) Error amplifier)

Do not use "Open/short protection at FB pin" as ON/OFF control by lowering FB pin voltage. In this case, there is a possibility of an abnormal rise of PFC output voltage at the turning on and off.

12. Example of application circuit



Note

This application circuit exemplifies the use of IC for your reference only. Parts tolerance, parts characteristics, influence of noise, etc. are not defined in this application circuit. When design an actual circuit for a product, you must determine parts tolerance, parts characteristics, influence of noise, etc. for safe and economical operation. Neither Fuji nor its agents shall be liable for any injury caused by any use of this circuit.