Enpirion® Power Datasheet

EC2630QI 4.5A, 27W 12V DC-DC Intermediate Voltage Bus Converter

Description

Altera's Enpirion EC2630QI is a high density DC-DC Intermediate Voltage Bus Converter which generates a highly efficient output voltage. EC2630QI that tracks one half the input voltage and is designed to work with Altera's highly integrated Enpirion DC to DC point-of-load converter products for a complete 12V solution. EC2630QI provides the means to condition power from a 12V input, to supply multiple lower voltage converters while enabling high efficiency and small PCB area. Due to its extremely high efficiency, it avoids the common two stage power conversion penalty and is equivalent or better than direct regulation.

This Altera Enpirion solution significantly helps in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, a reduction in the number of vendors required for the complete power solution helps to enable an overall system cost savings. All of Altera's Enpirion products are RoHS compliant and use a lead-free manufacturing environment.

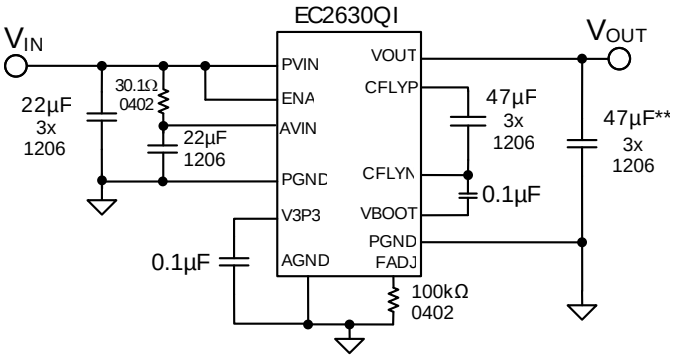


Figure 1: Typical Application Schematic Optimized for Maximum Efficiency

** 1-2 of Cout can be eliminated using downstream input bypass capacitance (e.g. PoL converters).

Features

- Complete power conditioning solution from a 12 volt power bus.
- Wide system input voltage range of 8V to 13.2V.
- High and flat efficiency, up to 97.5%.
- 4.5A Continuous Output Current Capability
- Adjustable operating frequency with optional external clock input.
- Master/Slave Mode for Parallel Operation
- Output Enable pin, VOUT_OK, VIN_OK
- Pre-programmed soft-start time.
- Thermal shutdown, short circuit, Overload, OVLO and UVLO protection.
- RoHS compliant, MSL level 3, 260C reflow.

Applications

- Applications requiring down conversion from a 12V bus to a well regulated output voltage with high efficiency, in a compact foot print (Note: The total system application involves two or more Altera Enpirion products.)
- Enterprise, Industrial, Embedded, and Telecommunication applications
- Multi-rail computer & network interface applications such as PCIe and ATCA AMC cards.
- 12V Industrial and Consumer Applications such as Audio/Video Home Theater, Tuners

Ordering Information

Part Number	Temp Rating (°C)	Package
EC2630QI	-40 to +85	36 pin 5.5 x5.5 QFN Package
EVB-EC2630QI	QFN Evaluation Board	

Pin Configuration

Below is a top view diagram of EC2630QI package.

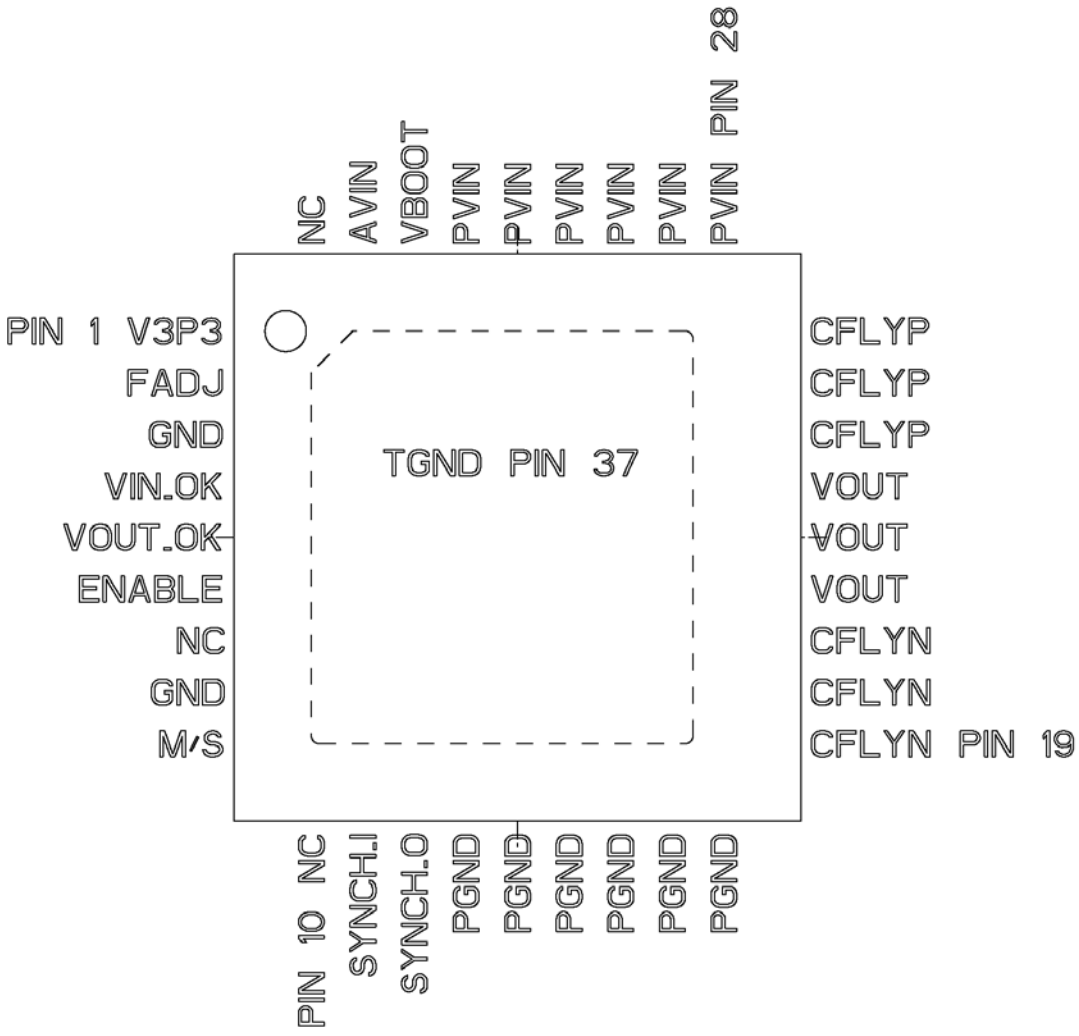


Figure 2: Pin-out diagram, top view of EC2630QI QFN Package.

NOTE: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. Failure to follow this guideline may result in damage to the Device.

NOTE: All pins must be soldered to PCB.

Pin Descriptions

PIN	NAME	FUNCTION
1	V3P3	Internal Regulated Supply Output. Connect bypass capacitor from V3P3 to GND.
2	FADJ	Frequency Adjust pin used to set the switching frequency. See Theory of Operation Section for selecting the required resistor.
3, 8	GND	Internal Regulated Supply Ground. Must tie directly to ground plane with a via right next to each pin.
4	VIN_OK	Vin OK is an open drain transistor for power system state indication for nominal 12V operation. VIN_OK is a logic high when Vin is greater than 9V.
5	VOUT_OK	VOUT_OK is an open drain transistor for power system state indication. VOUT_OK is a logic high when Vout is greater than 85% of expected nominal Vout. This pin should be used to control the ENABLE signals of downstream converters powered by the EC2630.
6	ENABLE	This pin should be tied to V_{IN} all the time. Contact Altera Power Applications support for more information.
7	NC	NO CONNECT — Do not electrically connect these pins to each other or to any other electrical signal. CAUTION: May be internally connected.
9	M/S	Master/Slave pin for clock synchronization. Logic low = Master. Logic high = Slave.
10	NC	NO CONNECT — Do not electrically connect these pins to each other or to any other electrical signal. CAUTION: May be internally connected.
11	SYNCH_I	External Synchronizing Clock Input, input accepted in Slave mode. From an IBC in master mode.
12	SYNCH_O	Synchronizing Clock Output. Frequency scaled output of internal oscillator.
13-18	PGND	Power ground for the switching voltage attenuator
19-21	CFLYN	Negative Terminal of Flying Capacitor
22-24	VOUT	Converter Output Voltage
25-27	CFLYP	Positive Terminal of Flying Capacitor
28-33	PVIN	Main Input Supply
34	VBOOT	Internal power Supply for high-side drive to which boot-strap capacitor is tied.
35	AVIN	Input Supply for Controller
36	NC	NO CONNECT – Do not electrically connect these pins to each other or to any other electrical signal. CAUTION: May be internally connected.
37	TGND	This pad is a thermal gnd. Needs to be thermally and electrically connected to the ground plane through a matrix of vias.

Block Diagram

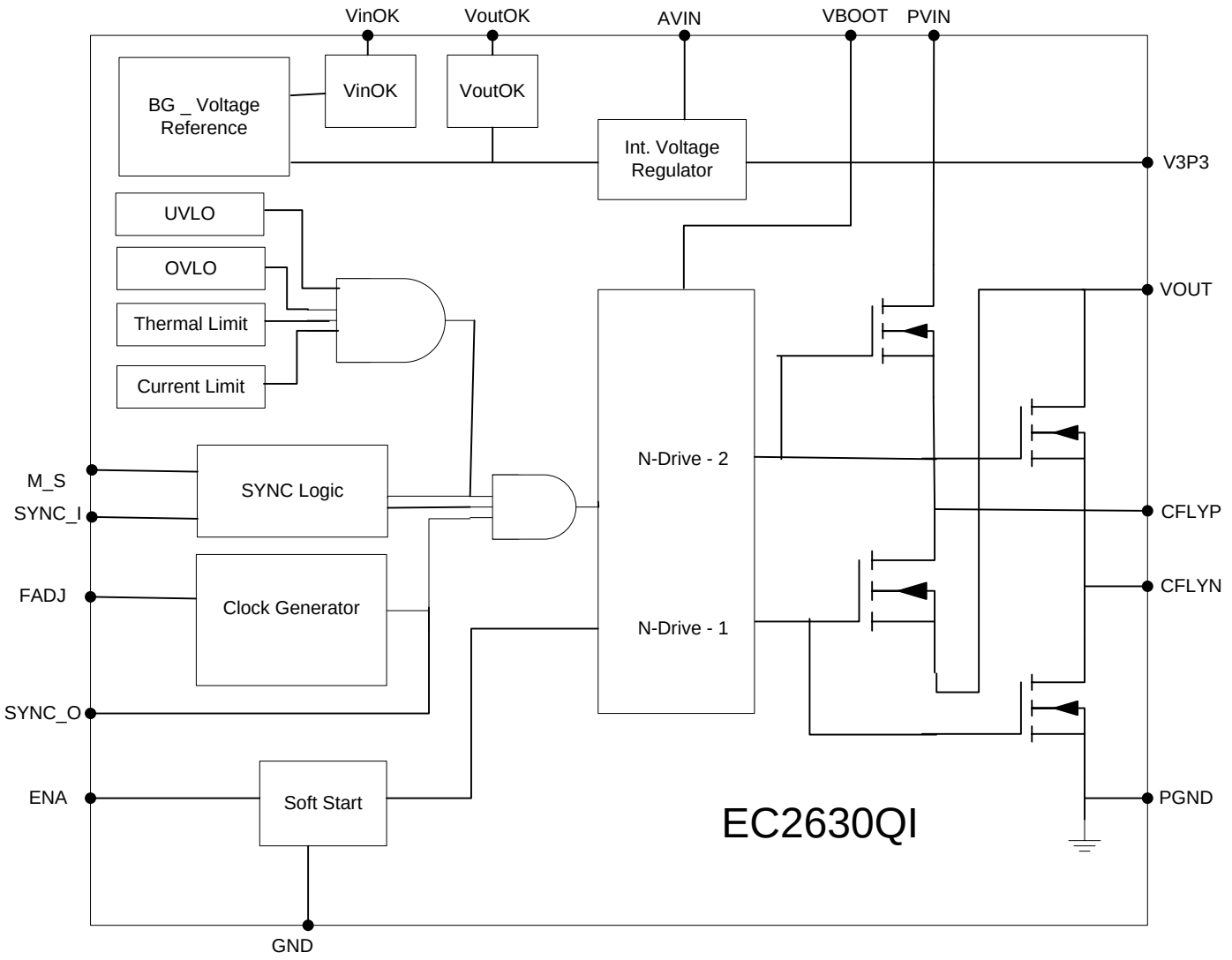


Figure 3: Block diagram.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond recommended operating conditions is not implied. Stress beyond absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Supply Voltage – PVIN, AVIN	V_{IN}	-0.5	15	V
Transient Input Supply Voltage, 2 ms maximum duration, 100 Hz repetition rate			20	V
Input Voltage – ENA, VIN_OK, VOUT_OK, CFLYN, CFLYP, Vout		-0.5	VIN	V
Input Voltage – V3P3, FADJ, M_S, SYNC_I, SYNC_O		-0.5	3.5	V
Input Voltage - VBOOT		-0.5	VIN + 8	V
Storage Temperature Range	T_{STG}	-65	150	°C
Maximum Operating Junction Temperature	$T_{J\text{-}ABS\_MAX}$		150	°C
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A			260	°C
ESD Rating (based on Human Body Model): AVIN	Positive Negative	1500 2000		V
ESD Rating (based on Human Body Model): All other pins		2000		V
ESD Rating (based on Charged Device Model)		500		V

Thermal Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Operating Junction Temp	T_J	-40		+125	°C
Thermal Shutdown	T_{SD}		155		°C
Thermal Shutdown Hysteresis	T_{SDH}		25		°C
Thermal Resistance: Junction to Case	θ_{JC}		1		°C/W
Thermal Resistance: Junction to Ambient	θ_{JA}		19		°C/W

Electrical Characteristics

NOTE: V_{IN}=12.0V over operating temperature range unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}		8	12	13.2	V
Operating Boot Strap Voltage	VBOOT	@ Vin =12V, with 0.1uF capacitor between VBOOT and CFLYN		17		V
Internal Regulated Supply Output	V3P3	@ Vin =12V	2.97	3.3	3.63	V
Under Voltage Lockout	V_{UVLO}		4.5	5	5.5	V
Input Voltage Indication Rising	VIN_OK			9		V
Input Voltage Indication Falling				8		V
Over Voltage Lockout	V_{OVLO}		13.35	14.2	15.05	V
No Load Operating Current	I_{OP}	@ 12V input and 125kHz switching		2		mA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Switching Frequency (Internal Oscillator)	F_{OSC}	$R_{FADJUST}$= 100 KΩ,	68	115	165	kHz
Frequency Adjust Voltage	FADJ			1.2		V
Output Voltage	V_{OUT}	Fraction of input voltage with no load current		50		%
Output Voltage Indication Threshold Rising	VOUT_OK	As a percentage of expected output voltage		85%		V
Output Voltage Indication Threshold Falling	VOUT_OK	As a percentage of expected output voltage		70%		V
Output Impedance	R_{OUT}	$\Delta V_{OUT}/\Delta I_{LOAD}$ $R_{FADJUST}$= 100 KΩ,		90		mΩ
Continuous Output Current	I_{OUT_Max}		0		4.5	A
Overload Trip Level	V_{OCP}	Vin=12V, Overload sensed as a drop in output voltage		5.2		V
Enable Threshold Logic Low	ENA_VIL	Max voltage to ensure the converter is disabled			0.3	V
Enable Threshold Logic High	ENA_VIH	6V ≤ V_{IN} ≤ 13.2V	1.8		V_{IN}	V
Logic Threshold Low M_S	VIL		-0.3		0.3	V
Logic Threshold High M_S	VIH		V3P3 - 0.6	V3P3	V3P3 + 0.3	V
External Clock frequency	F_{EXT}		0.01		1	MHz
Clock Input Logic Low	SYNC_I_VIL				0.3	V
Clock Input Logic High	SYNC_I_VIH		1.8		3.3	V
Clock Output Logic Low	SYNC_O_VOL				0.3	V
Clock Output Logic High	SYNC_O_VOH	@ 1mA	V3P3 - 0.6			V
VIN_OK, VOUT_OK sink capability		POK low voltage = 0.1V		1		mA

Typical Performance Characteristics

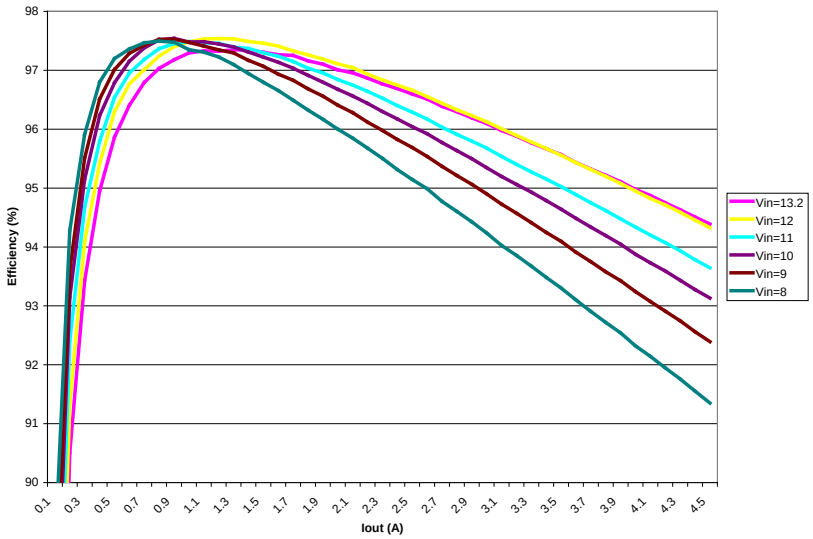


Fig. 4: Nominal Efficiency (%) vs. Load (A)
@ VIN = 13.2/12/10/8V, C_{IN}=3x22uF, C_{OUT}=3X47uF, C_{FLY}=3x47uF with $R_{FADJUST}$= 100 KΩ,

Start-up / Shutdown Wave forms with Enable tied to VIN

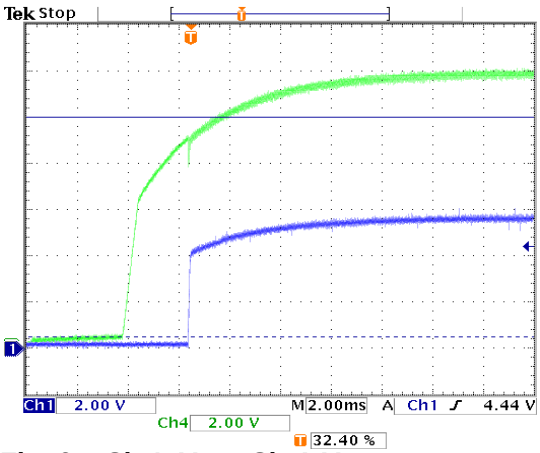


Fig. 6a: Ch.1: V_{OUT}, Ch.4: V_{IN}

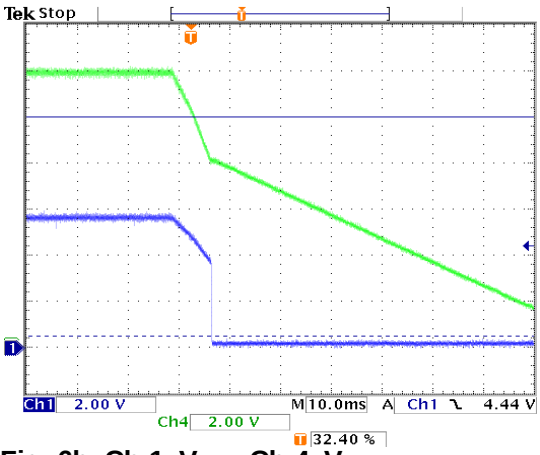


Fig. 6b: Ch.1: V_{OUT}, Ch.4: V_{IN}

Theory of Operation

Bus Voltage Divider

The EC2630QI is an open loop voltage divider. It generates an output voltage which is approximately half the input voltage value. The device uses switched capacitors to divide the input voltage by a factor of 2. External capacitors are charged in series during one half of a clock cycle and the capacitors are then connected in parallel during the second half of the clock cycle. Since there is no feedback to regulate the output voltage, the output voltage depends on the input voltage as well as the load current. Temperature dependence is a function of load current.

This device has been designed specifically for use along with Altera's Enpirion point-of-load products for output voltage regulation.

The Voltage Divider has the following features:

- Over-current protection (to protect the IC from excessive load current)
- Thermal shutdown with hysteresis.
- Under-voltage lockout circuit to disable the converter output when the input voltage is less than approximately 5V
- Over-voltage lockout circuit to disable the converter output when the input voltage is greater than approximately 14.2V
- Switching frequency is internally generated. However, a clock signal may be applied externally when the device is configured in Slave mode.
- When in Master mode, the device will output its internal frequency scaled clock to the SYNCH_O pin.
- Soft-start circuit, to limit the in-rush current when the converter is powered up.
- VIN_OK and VOUT_OK indicator signals.

Enable Operation

A logic high on this pin will turn the device on, and logic low will disable the output. Under normal operation, the ENABLE pin needs to be tied to PVIN. The device is then turned on and off by ramping the input voltage up and down. Contact Altera Power Applications support for further details.

Frequency Synch (Master/Slave)

In Slave mode, an external clock may be used for switching the bus converter by connecting such a source to SYNC_I pin when the device is configured. In Master mode, the internal switching frequency of the Master device is outputted through SYNCH_O pin. This clock signal can be used to drive other EC2630QI devices for synchronization or parallel operation.

Soft-Start Operation

Soft start is a means to reduce the in-rush current when the device is enabled. When the device is enabled by ramping up the input voltage, and the output capacitors are discharged, a large current flow is averted by modulating the gate drive of the NFET during the soft start interval. This interval is pre-programmed and not user programmable.

Overload Protection

The overload function is achieved by sensing the output voltage. An overload state is entered when the device is out of soft start and the output voltage drops below ~85% of the expected voltage. This overload state will initiate a fresh soft-start and the device will stay looping in soft-start as long as the overload condition exists.

Over-Voltage Protection

When the input voltage exceeds 14.2V, the flying capacitor is placed in parallel with the output capacitor during OVLO and the device does not switch.

Thermal Overload Protection

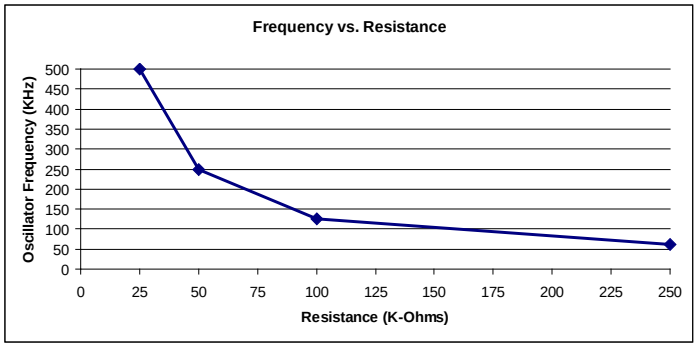
Thermal shutdown will disable operation when the Junction temperature exceeds the value given in the Electrical Characteristics table. Once the junction temperature drops by the hysteresis temperature, the converter will re-start with a normal soft-start.

Input Under-voltage Lock-out

Internal circuits ensure that the converter will not start switching until the input voltage is above the specified minimum voltage of ~5V.

Frequency Adjustment

The device is optimized to run at 125kHz switching frequency (with R_{FADJ}= 100 KΩ) independent of load current. The internal oscillator frequency can be adjusted by altering the value of the resistor between the FADJ pin and AGND (see chart below). Contact Altera Power Applications support for further details.



Application Schematic

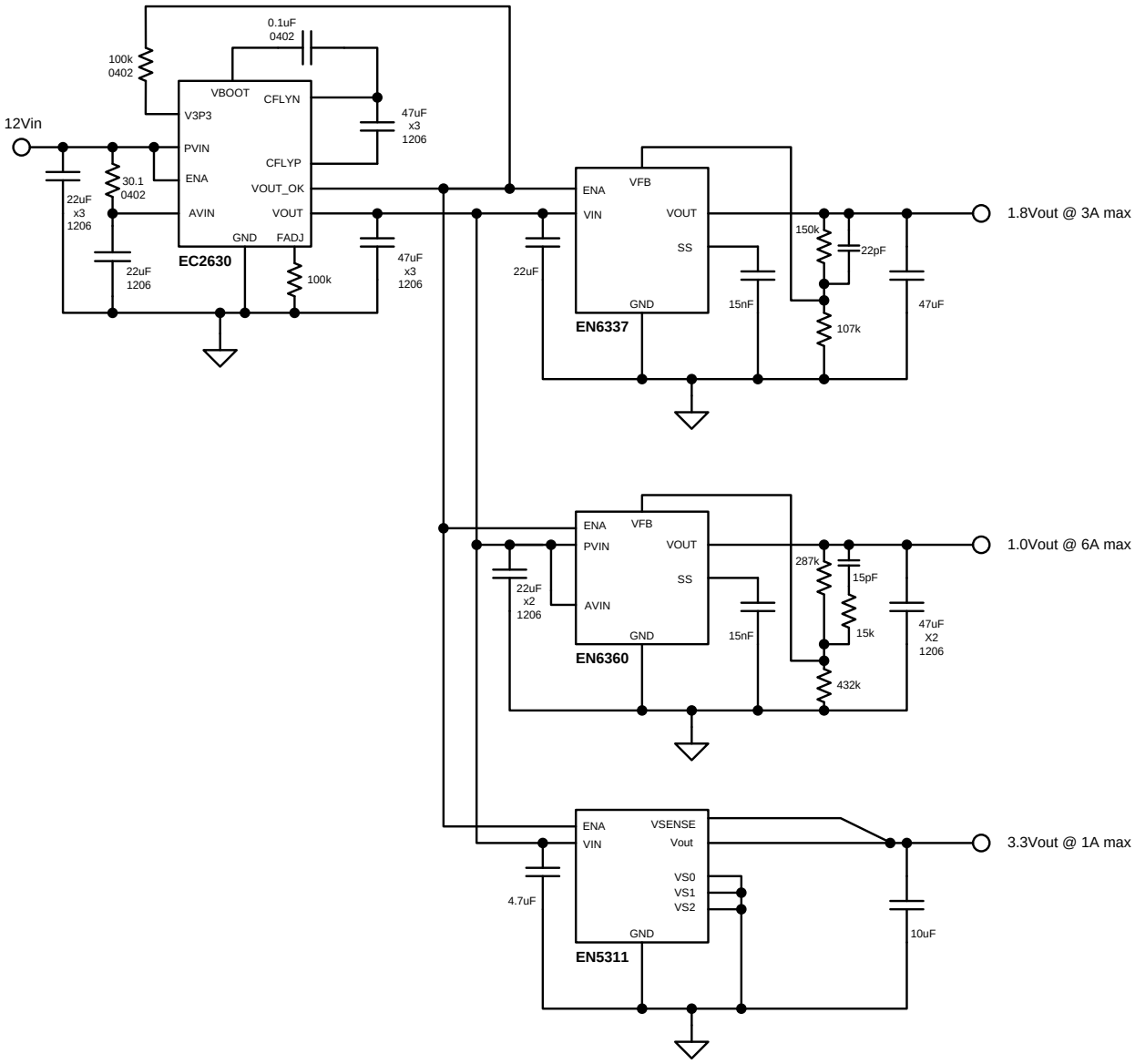


Figure 7: EC2630 connected to a 12V input supply supplying 3 point-of-load Altera Enpirion DC-DC switchers.

Figure 7 shows a typical application where the EC2630 is powering up three downstream Altera Enpirion point-of-load (POL) converters. As shown in Figure 7, the EC2630 VOUT_OK signal should be used to control the ENABLE pins of the downstream converters. This ensures that the intermediate bus voltage is up before the POL converters start switching. In addition please use only POL converters rated for up to 6.6V input voltage operation.

Capacitor Selection

The EC2630QI requires a range of capacitance depending on application configuration. Capacitor selection is dependent upon power level, efficiency, space, and cost requirements. Low-cost, low-ESR X5R or X7R ceramic capacitors should be used. Either 1206 or 1210 case sizes are recommended. In general, 1210 capacitors exhibit less voltage coefficient than 1206 capacitors, providing more capacitance per unit volume-volt. Y5V or equivalent dielectric formulations must not be used as they lose capacitance with frequency, temperature and bias voltage.

Capacitor selection guidelines to support full output load (4.5A) optimized for efficiency:

- Input Capacitors- a typical implementation might use 3x22µF, 1206 MLCC capacitors
- Output Capacitors- a typical implementation might use 3X47µF, 1206 output
- Flying Capacitors- a typical implementation might use 3x47µF 1206.
- A portion of the output capacitance or flying capacitance can be allocated to the underside of the board. In addition, a portion of Cout can be shared with downstream input bypass capacitance (e.g. PoL converters).

Optional External Over-Current Protection (OCP)

For some applications, output load levels that drive the EC2630 into very high-current conditions with VOUT at nominal $V_{IN}/2$ voltages can lead to EC2630 device damage. Altera has observed that high-current conditions over 6A - while VOUT is regulating at $V_{IN}/2$ - can lead to device failure. When the EC2630 fails, the device will stop regulating to $V_{OUT}=V_{IN}/2$, and the output will drop to approximately 2V. A failure event has not been found to damage downstream devices since V_{OUT} drops during the event. When an EC2630 device fails, it draws excessive current from the 12V input supply at its PVIN pin.

Figure 8 shows a recommended circuit for external over-current protection. Applications that implement other means of over-current and short-circuit protection by using other supervisory or control circuits do not need to use the circuit shown in Figure 8. Please contact Altera Power Applications support for more details.

This circuit interfaces to the following pins on the EC2630: AVIN, FADJ, ENABLE, VOUTOK, and GND. It uses the VOUT_OK signal to decide if there is an over-current condition. If VOUT_OK is high, then the circuit allows the EC2630 to operate normally. As soon as VOUT_OK goes to a logic low, it is interpreted as an over-current condition, and the circuit lowers the device operating frequency, and causes it to go into a hiccup mode. The hiccup mode continues indefinitely until VOUT_OK goes high.

There are two timers in this circuit. C1 and its associated resistors sets up a soft-start timer, and C2 and its associated resistors set up a hiccup timer. The active components in this circuit were chosen based on device availability. Similar components can be used as long as the performance is comparable to the ones shown in Figure 8. Please note the circuit also requires an external 3.3V, low-current rail.

If an over-current or short-circuit condition is encountered while using the circuit of Figure 8 with the EC2630, leave the power on for at least 2 seconds before turning it off, and wait an additional 2 seconds before re-applying power.

Please note when using the circuit of Figure 8, the EC2630 ENABLE pin is not tied to VIN any more. This pin needs be toggled by the circuit for proper OCP operation.

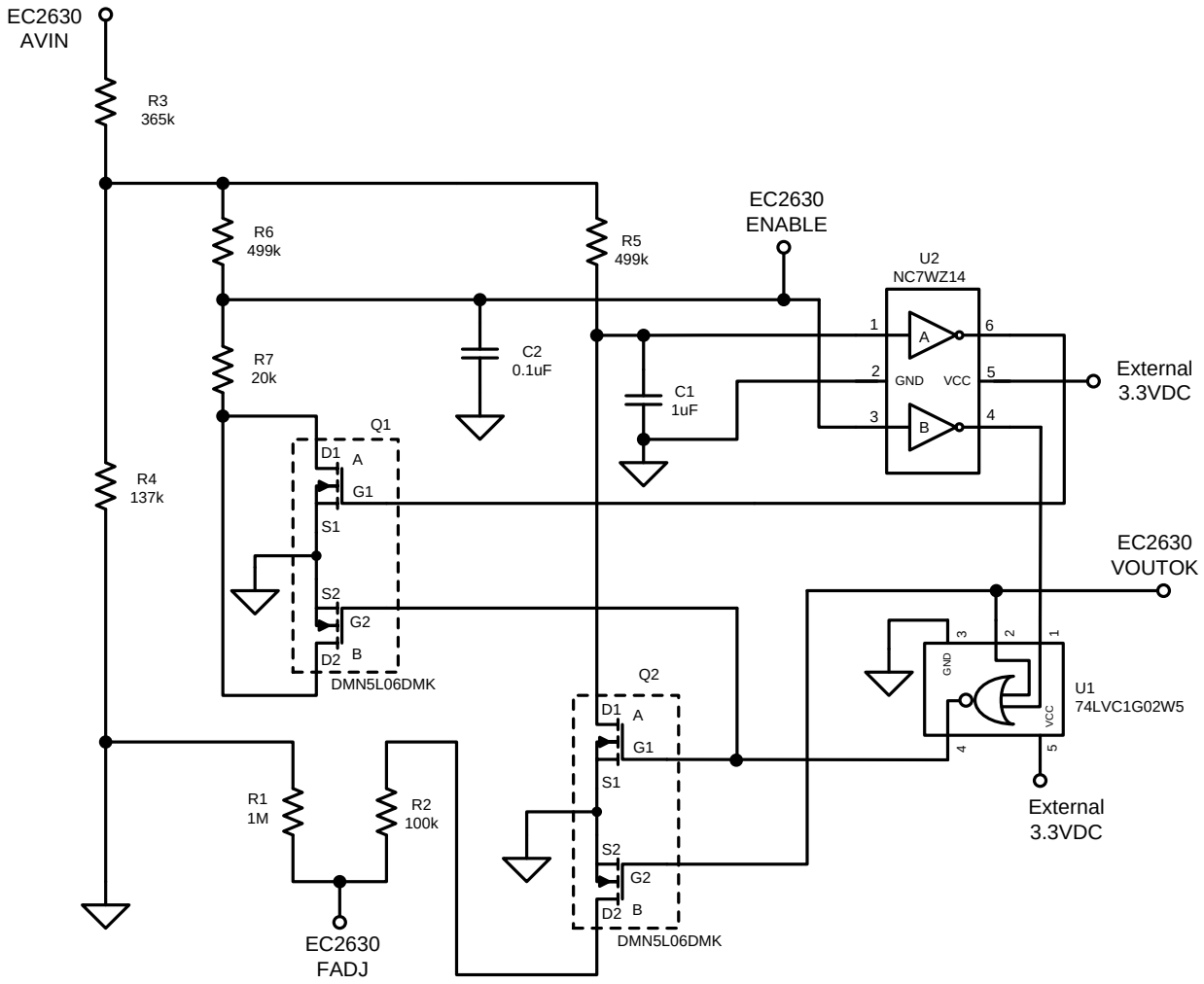


Figure 8: Optional External Over-Current Protection Circuit

Mechanical Information

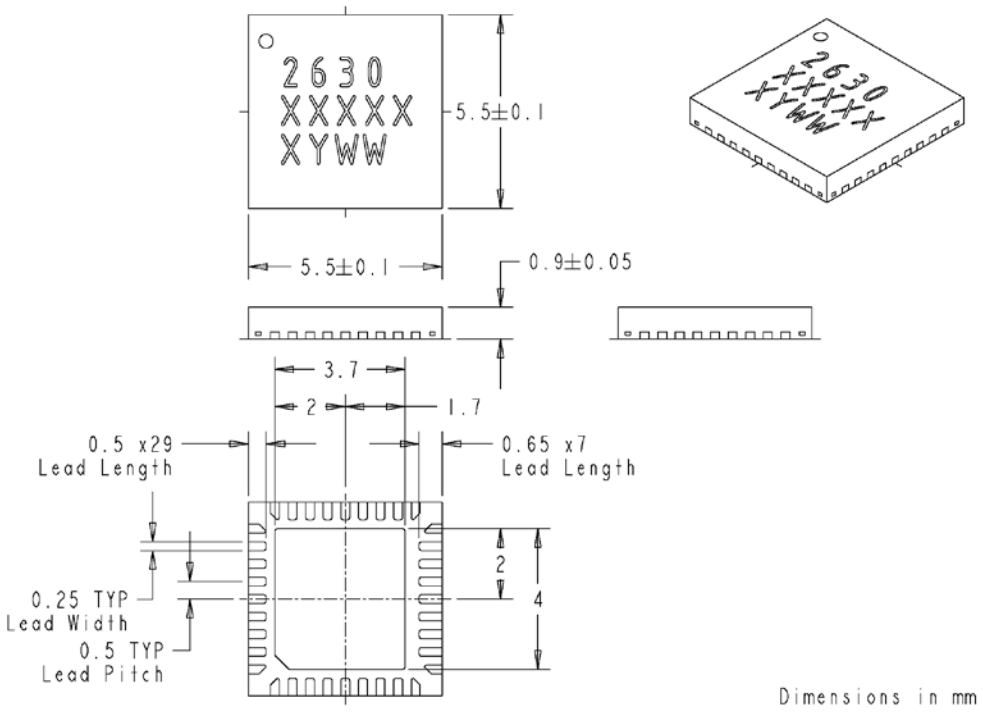


Figure 9: EC2630 Package Dimensions

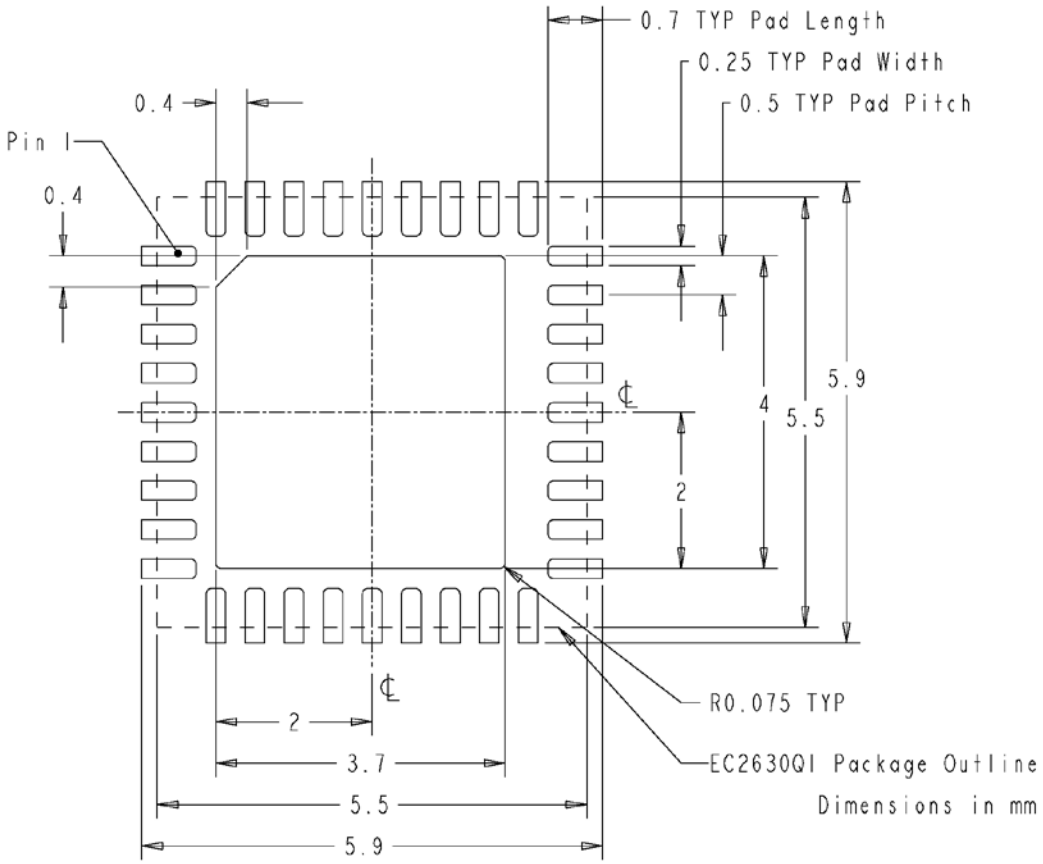


Figure 10: Recommended PCB footprint.

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