

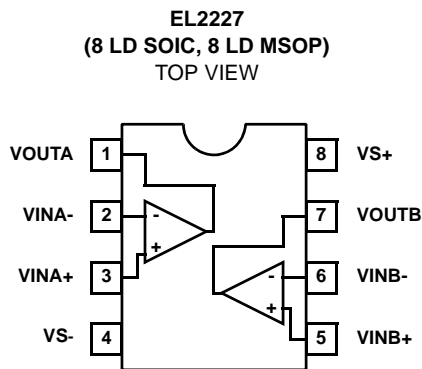
## Dual Very Low Noise Amplifier

The EL2227 is a dual, low-noise amplifier, ideally suited to line receiving applications in ADSL and HDSLII designs. With low noise specification of just 1.9nV/√Hz and 1.2pA/√Hz, the EL2227 is perfect for the detection of very low amplitude signals.

The EL2227 features a -3dB bandwidth of 115MHz and is gain-of-2 stable. The EL2227 also affords minimal power dissipation with a supply current of just 4.8mA per amplifier. The amplifier can be powered from supplies ranging from ±2.5V to ±12V.

The EL2227 is available in a space-saving 8 Ld MSOP package as well as the industry-standard 8 Ld SOIC. It can operate over the -40°C to +85°C temperature range.

### Pinout



### Features

- Voltage noise of only 1.9nV/√Hz
- Current noise of only 1.2pA/√Hz
- Bandwidth (-3dB) of 115MHz @ $A_V = +2$
- Gain-of-2 stable
- Just 4.8mA per amplifier
- 8 Ld MSOP package
- ±2.5V to ±12V operation
- Pb-free plus anneal available (RoHS compliant)

### Applications

- ADSL receivers
- HDSLII receivers
- Ultrasound input amplifiers
- Wideband instrumentation
- Communications equipment
- AGC and PLL active filters
- Wideband sensors

### Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	TAPE AND REEL	PACKAGE	PKG. DWG.#
EL2227CY	L	-40 to +85	-	8 Ld MSOP (3.0mm)	MDP0043
EL2227CY-T13	L	-40 to +85	13"	8 Ld MSOP (3.0mm)	MDP0043
EL2227CY-T7	L	-40 to +85	7"	8 Ld MSOP (3.0mm)	MDP0043
EL2227CYZ (Note)	BASAA	-40 to +85	-	8 Ld MSOP (3.0mm) (Pb-free)	MDP0043
EL2227CYZ-T13 (Note)	BASAA	-40 to +85	13"	8 Ld MSOP (3.0mm) (Pb-free)	MDP0043
EL2227CYZ-T7 (Note)	BASAA	-40 to +85	7"	8 Ld MSOP (3.0mm) (Pb-free)	MDP0043
EL2227CS	2227CS	-40 to +85	-	8 Ld SOIC (150 mil)	MDP0027
EL2227CS-T13	2227CS	-40 to +85	13"	8 Ld SOIC (150 mil)	MDP0027
EL2227CS-T7	2227CS	-40 to +85	7"	8 Ld SOIC (150 mil)	MDP0027
EL2227CSZ (Note)	2227CSZ	-40 to +85	-	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL2227CSZ-T13 (Note)	2227CSZ	-40 to +85	13"	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL2227CSZ-T7 (Note)	2227CSZ	-40 to +85	7"	8 Ld SOIC (150 mil) (Pb-free)	MDP0027

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

**Absolute Maximum Ratings**

Supply Voltage between $V_{S+}$ and $V_{S-}$ .....	.28V
Input Voltage .....	$V_{S-} - 0.3V, V_{S+} + 0.3V$
Maximum Continuous Output Current .....	40mA
Maximum Die Temperature .....	+150°C
ESD Voltage.....	.2kV

**Thermal Information**

Storage Temperature .....	-65°C to +150°C
Operating Temperature .....	-40°C to +85°C
Power Dissipation .....	See Curves
Pb-free reflow profile .....	see link below
	<a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**IMPORTANT NOTE:** All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$

**Electrical Specifications**  $V_{S+} = +12V, V_{S-} = -12V, R_L = 500\Omega$  and  $C_L = 3pF$  to 0V,  $R_F = R_G = 620\Omega$ , and  $T_A = +25^\circ C$  Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
<b>INPUT CHARACTERISTICS</b>						
$V_{OS}$	Input Offset Voltage	$V_{CM} = 0V$		-0.2	3	mV
$TCV_{OS}$	Average Offset Voltage Drift			-0.6		$\mu V/^\circ C$
$I_B$	Input Bias Current	$V_{CM} = 0V$	-9	-3.4		$\mu A$
$R_{IN}$	Input Impedance			7.3		$M\Omega$
$C_{IN}$	Input Capacitance			1.6		pF
CMIR	Common-Mode Input Range		-11.8		+10.4	V
CMRR	Common-Mode Rejection Ratio	for $V_{IN}$ from -11.8V to 10.4V	60	94		dB
$A_{VOL}$	Open-Loop Gain	$-5V \leq V_{OUT} \leq 5V$	70	87		dB
$e_N$	Voltage Noise	$f = 100kHz$		1.9		$nV/\sqrt{Hz}$
$i_N$	Current Noise	$f = 100kHz$		1.2		$pA/\sqrt{Hz}$
<b>OUTPUT CHARACTERISTICS</b>						
$V_{OL}$	Output Swing Low	$R_L = 500\Omega$		-10.4	-10	V
		$R_L = 250\Omega$		-9.8	-9	V
$V_{OH}$	Output Swing High	$R_L = 500\Omega$	10	10.4		V
		$R_L = 250\Omega$	9.5	10		V
$I_{SC}$	Short Circuit Current	$R_L = 10\Omega$	140	180		mA
<b>POWER SUPPLY PERFORMANCE</b>						
PSRR	Power Supply Rejection Ratio	$V_S$ is moved from $\pm 2.25V$ to $\pm 12V$	65	95		dB
$I_S$	Supply Current (Per Amplifier)	No Load		4.8	6.5	mA
$V_S$	Operating Range		$\pm 2.5$		$\pm 12$	V
<b>DYNAMIC PERFORMANCE</b>						
SR	Slew Rate (Note 2)	$\pm 2.5V$ square wave, measured 25% to 75%	40	50		$V/\mu S$
$t_S$	Settling to 0.1% ( $A_V = +2$ )	( $A_V = +2$ ), $V_O = \pm 1V$		65		ns
BW	-3dB Bandwidth	$R_F = 358\Omega$		115		MHz
HD2	2nd Harmonic Distortion	$f = 1MHz, V_O = 2V_{P-P}, R_L = 500\Omega, R_F = 358\Omega$		93		dBc
		$f = 1MHz, V_O = 2V_{P-P}, R_L = 150\Omega, R_F = 358\Omega$		83		dBc
HD3	3rd Harmonic Distortion	$f = 1MHz, V_O = 2V_{P-P}, R_L = 500\Omega, R_F = 358\Omega$		94		dBc
		$f = 1MHz, V_O = 2V_{P-P}, R_L = 150\Omega, R_F = 358\Omega$		76		dBc

**Electrical Specifications**  $V_{S+} = +12V$ ,  $V_{S-} = -12V$ ,  $R_L = 500\Omega$  and  $C_L = 3pF$  to 0V,  $R_F = R_G = 620\Omega$ , and  $T_A = +25^\circ C$  Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
<b>INPUT CHARACTERISTICS</b>						
$V_{OS}$	Input Offset Voltage	$V_{CM} = 0V$		0.2	3	mV
$TCV_{OS}$	Average Offset Voltage Drift			-0.6		$\mu V/^\circ C$
$I_B$	Input Bias Current	$V_{CM} = 0V$	-9	-3.7		$\mu A$
$R_{IN}$	Input Impedance			7.3		$M\Omega$
$C_{IN}$	Input Capacitance			1.6		pF
CMIR	Common-Mode Input Range		-4.8		3.4	V
CMRR	Common-Mode Rejection Ratio	for $V_{IN}$ from -4.8V to 3.4V	60	97		dB
$A_{VOL}$	Open-Loop Gain	$-5V \leq V_{OUT} \leq 5V$	70	84		dB
$e_N$	Voltage Noise	$f = 100kHz$		1.9		$nV/\sqrt{Hz}$
$i_N$	Current Noise	$f = 100kHz$		1.2		$pA/\sqrt{Hz}$
<b>OUTPUT CHARACTERISTICS</b>						
$V_{OL}$	Output Swing Low	$R_L = 500\Omega$		-3.8	-3.5	V
		$R_L = 250\Omega$		-3.7	-3.5	V
$V_{OH}$	Output Swing High	$R_L = 500\Omega$	3.5	3.7		V
		$R_L = 250\Omega$	3.5	3.6		V
$I_{SC}$	Short Circuit Current	$R_L = 10\Omega$	60	100		mA
<b>POWER SUPPLY PERFORMANCE</b>						
PSRR	Power Supply Rejection Ratio	$V_S$ is moved from $\pm 2.25V$ to $\pm 12V$	65	95		dB
$I_S$	Supply Current (Per Amplifier)	No Load		4.5	5.5	mA
$V_S$	Operating Range		$\pm 2.5$		$\pm 12$	V
<b>DYNAMIC PERFORMANCE</b>						
SR	Slew Rate	$\pm 2.5V$ square wave, measured 25%-75%	35	45		$V/\mu S$
$t_S$	Settling to 0.1% ( $A_V = +2$ )	( $A_V = +2$ ), $V_O = \pm 1V$		77		ns
BW	-3dB Bandwidth	$R_F = 358\Omega$		90		MHz
HD2	2nd Harmonic Distortion	$f = 1MHz$ , $V_O = 2V_{P-P}$ , $R_L = 500\Omega$ , $R_F = 358\Omega$		98		dBc
		$f = 1MHz$ , $V_O = 2V_{P-P}$ , $R_L = 150\Omega$ , $R_F = 358\Omega$		90		dBc
HD3	3rd Harmonic Distortion	$f = 1MHz$ , $V_O = 2V_{P-P}$ , $R_L = 500\Omega$ , $R_F = 358\Omega$		94		dBc
		$f = 1MHz$ , $V_O = 2V_{P-P}$ , $R_L = 150\Omega$ , $R_F = 358\Omega$		79		dBc

Typical Performance Curves

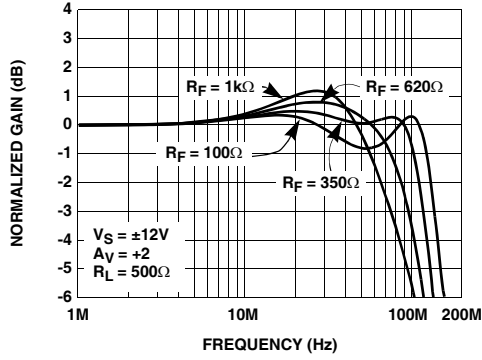


FIGURE 1. NON-INVERTING FREQUENCY RESPONSE FOR VARIOUS  $R_F$

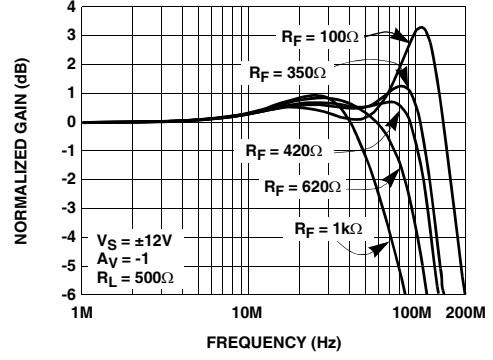


FIGURE 2. INVERTING FREQUENCY RESPONSE FOR VARIOUS  $R_F$

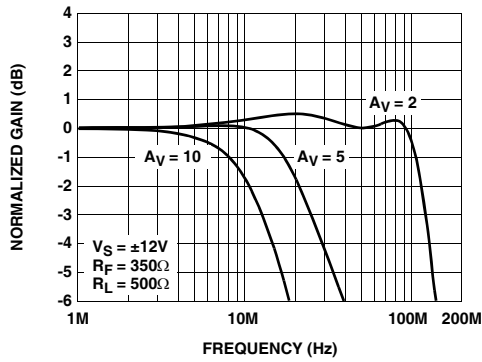


FIGURE 3. NON-INVERTING FREQUENCY RESPONSE (GAIN)

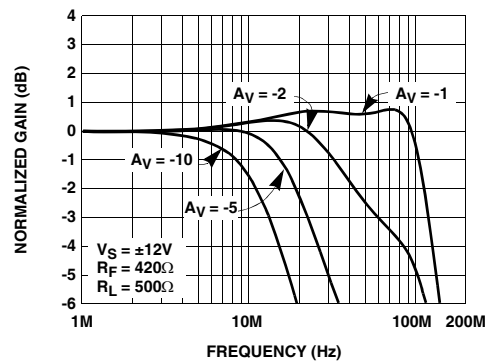


FIGURE 4. INVERTING FREQUENCY RESPONSE (GAIN)

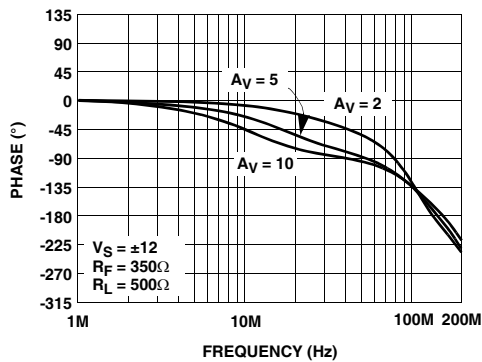


FIGURE 5. NON-INVERTING FREQUENCY RESPONSE (PHASE)

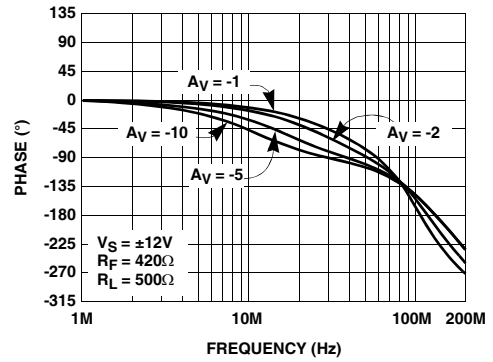


FIGURE 6. INVERTING FREQUENCY RESPONSE (PHASE)

Typical Performance Curves (Continued)

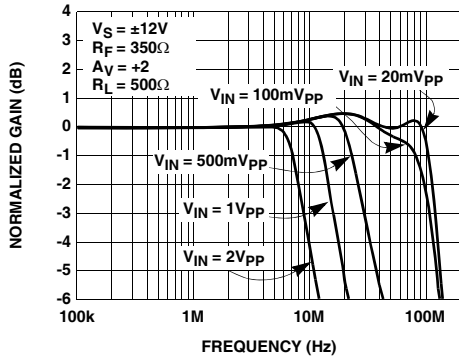


FIGURE 7. NON-INVERTING FREQUENCY RESPONSE FOR VARIOUS INPUT SIGNAL LEVELS

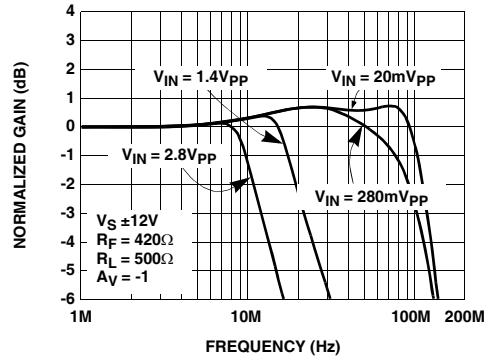


FIGURE 8. INVERTING FREQUENCY RESPONSE FOR VARIOUS INPUT SIGNAL LEVELS

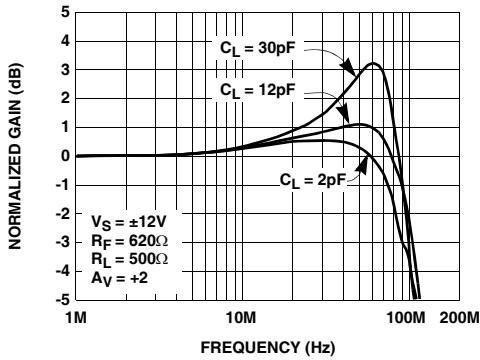


FIGURE 9. NON-INVERTING FREQUENCY RESPONSE FOR VARIOUS C<sub>L</sub>

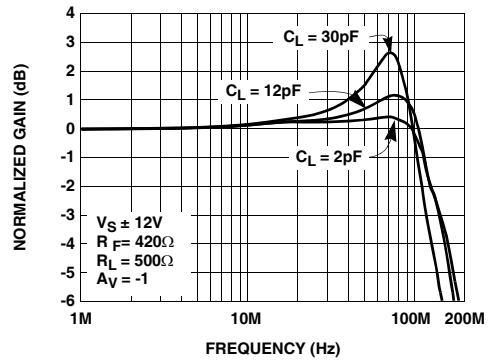


FIGURE 10. INVERTING FREQUENCY RESPONSE FOR VARIOUS C<sub>L</sub>

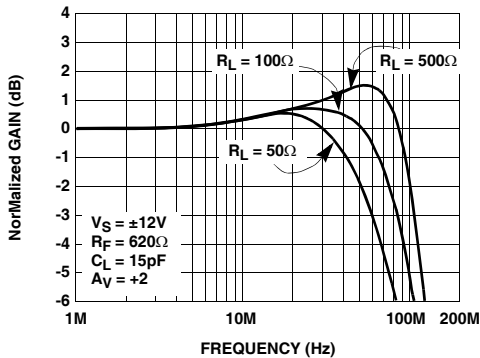


FIGURE 11. NON-INVERTING FREQUENCY RESPONSE FOR VARIOUS R<sub>L</sub>

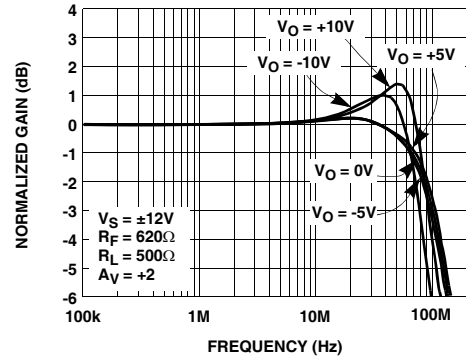


FIGURE 12. FREQUENCY RESPONSE FOR VARIOUS OUTPUT DC LEVELS

Typical Performance Curves (Continued)

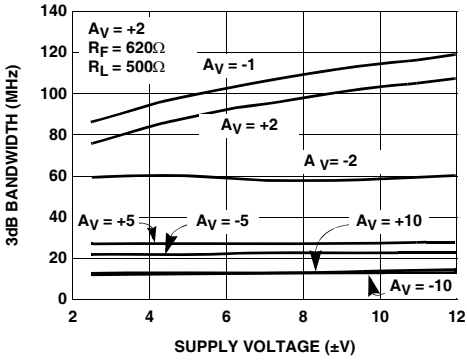


FIGURE 13. 3dB BANDWIDTH vs SUPPLY VOLTAGE

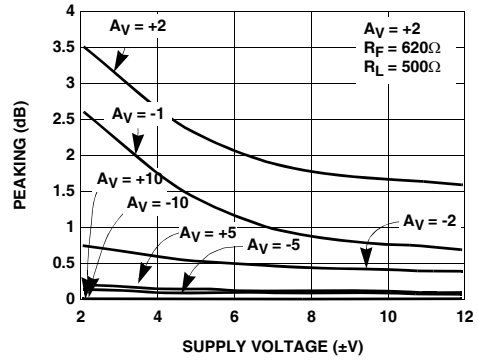


FIGURE 14. PEAKING vs SUPPLY VOLTAGE

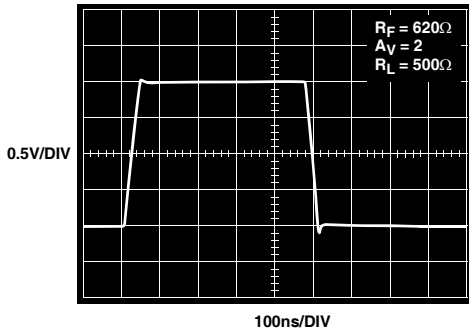


FIGURE 15. LARGE SIGNAL STEP RESPONSE (VS = ±12V)

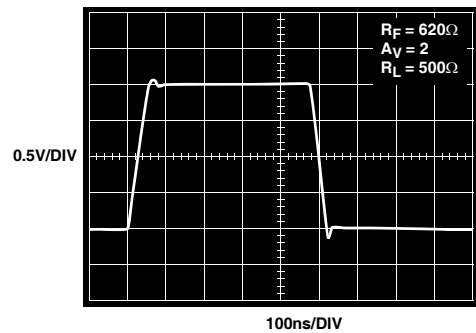


FIGURE 16. LARGE SIGNAL STEP RESPONSE (VS = ±2.5V)

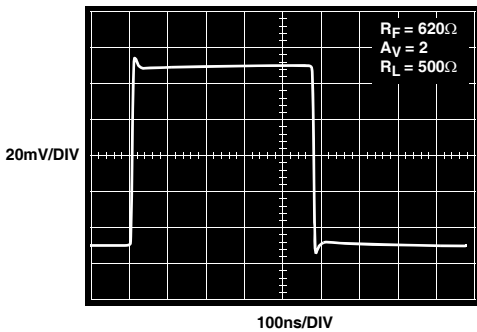


FIGURE 17. SMALL SIGNAL STEP RESPONSE (VS = ±12V)

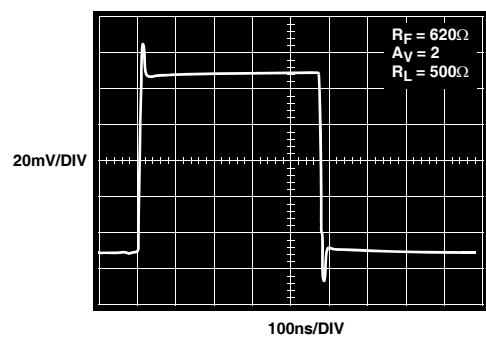


FIGURE 18. SMALL SIGNAL STEP RESPONSE (VS = ±2.5V)

Typical Performance Curves (Continued)

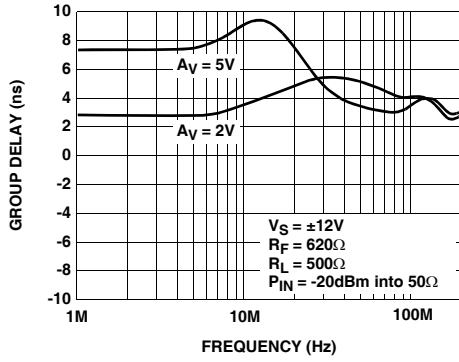


FIGURE 19. GROUP DELAY vs FREQUENCY

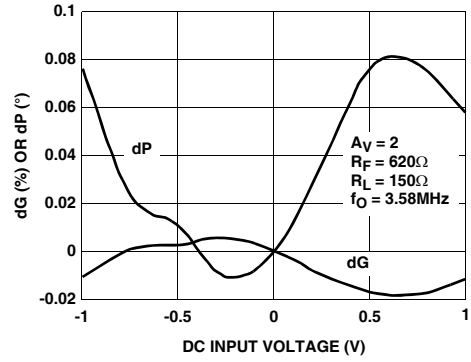


FIGURE 20. DIFFERENTIAL GAIN/PHASE vs DC INPUT VOLTAGE AT 3.58MHz

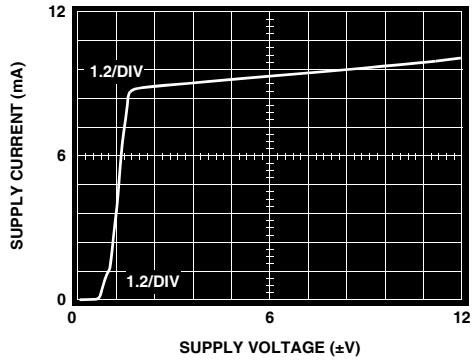


FIGURE 21. SUPPLY CURRENT vs SUPPLY VOLTAGE

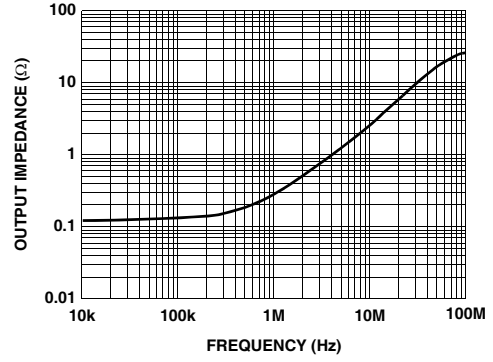


FIGURE 22. CLOSED LOOP OUTPUT IMPEDANCE vs FREQUENCY

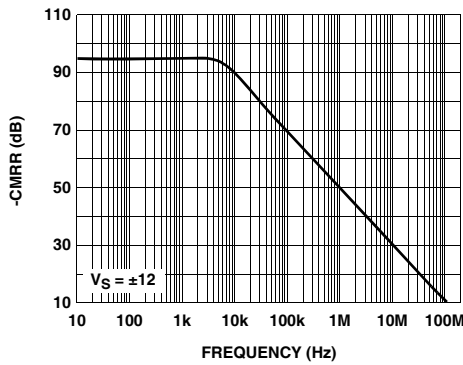


FIGURE 23. CMRR

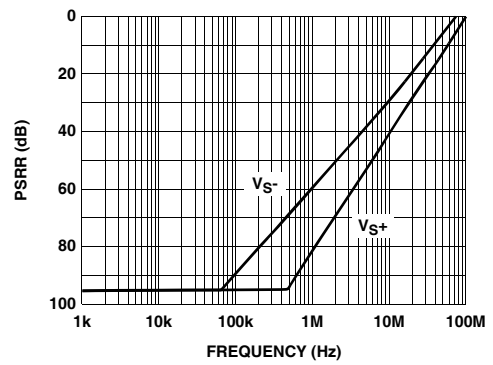


FIGURE 24. PSRR

Typical Performance Curves (Continued)

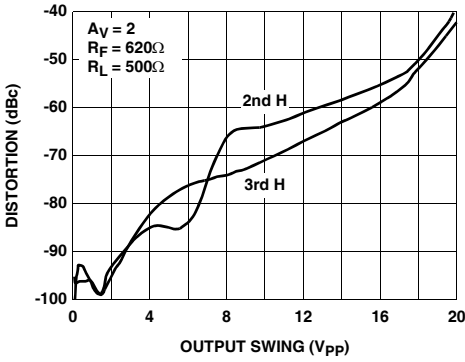


FIGURE 25. 1MHz 2nd and 3rd HARMONIC DISTORTION vs OUTPUT SWING FOR VS = ±12V

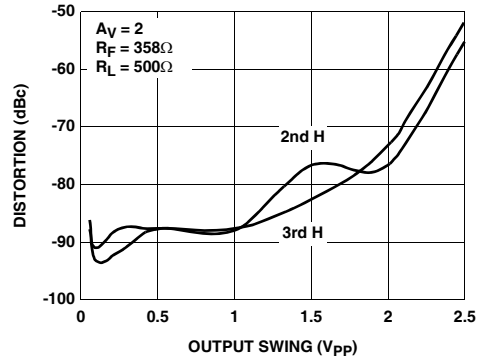


FIGURE 26. 1MHz 2nd and 3rd HARMONIC DISTORTION vs OUTPUT SWING FOR VS = ±2.5V

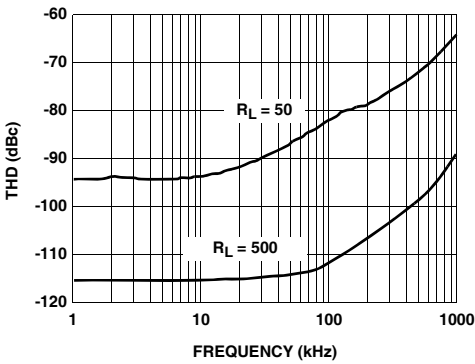


FIGURE 27. TOTAL HARMONIC DISTORTION vs FREQUENCY @ 2Vpp VS = ±12V

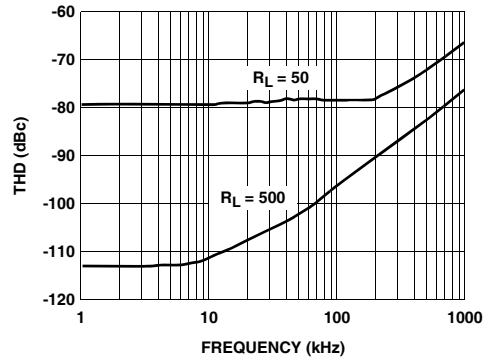


FIGURE 28. TOTAL HARMONIC DISTORTION vs FREQUENCY @ 2Vpp VS = ±2.5V

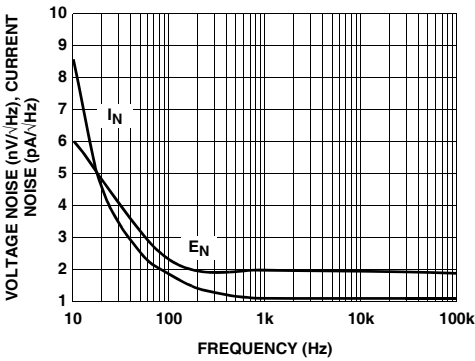


FIGURE 29. VOLTAGE AND CURRENT NOISE vs FREQUENCY

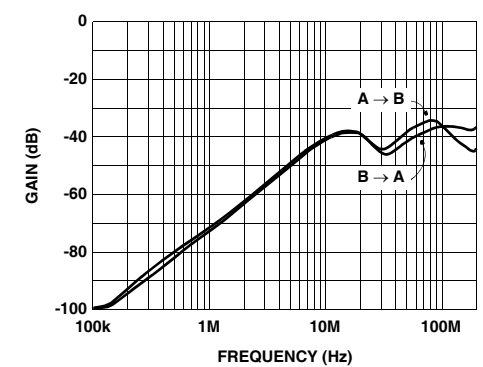


FIGURE 30. CHANNEL TO CHANNEL ISOLATION vs FREQUENCY



Typical Performance Curves (Continued)

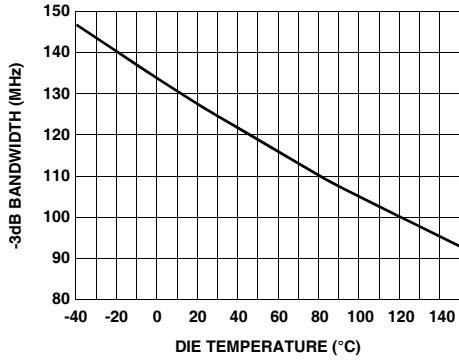


FIGURE 31. -3dB BANDWIDTH vs TEMPERATURE

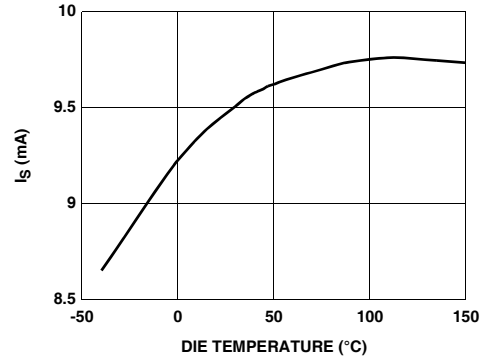


FIGURE 32. SUPPLY CURRENT vs TEMPERATURE

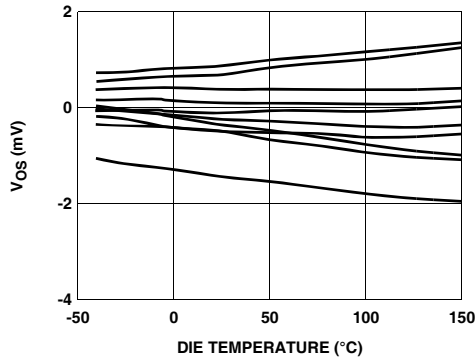


FIGURE 33. V<sub>OS</sub> vs TEMPERATURE

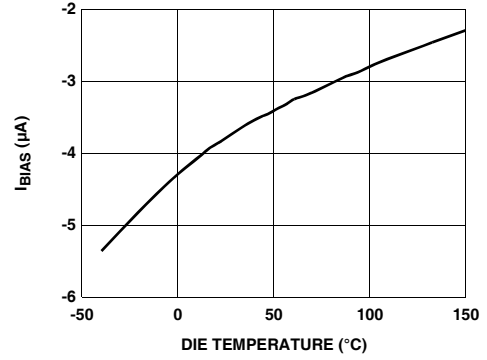


FIGURE 34. INPUT BIAS CURRENT vs TEMPERATURE

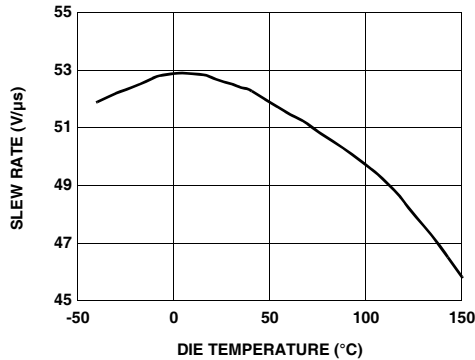


FIGURE 35. SLEW RATE vs TEMPERATURE

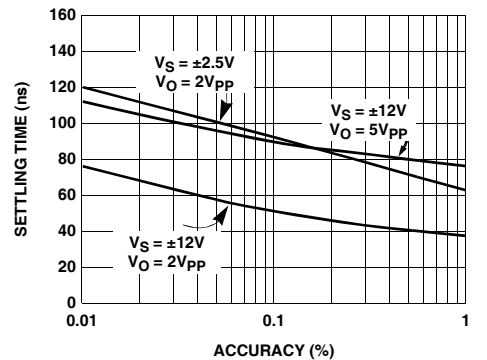


FIGURE 36. SETTLING TIME vs ACCURACY

Typical Performance Curves (Continued)

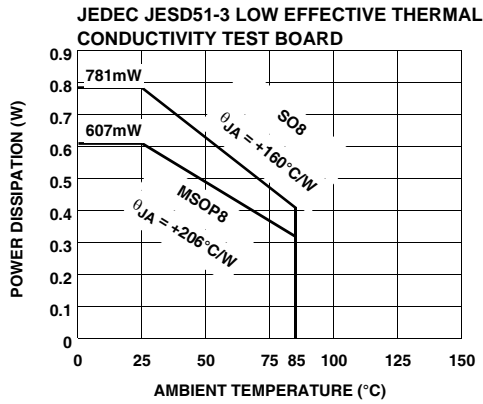


FIGURE 37. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Pin Descriptions

EL2227CY 8-PIN MSOP	EL2227CS 8-PIN SO	PIN NAME	PIN FUNCTION	EQUIVALENT CIRCUIT
1	1	VOUTA	Output	<p>Circuit 1</p>
2	2	VINA-	Input	<p>Circuit 2</p>
3	3	VINA+	Input	Reference Circuit 2
4	4	VS-	Supply	
5	5	VINB+	Input	
6	6	VINB-	Input	Reference Circuit 2
7	7	VOUTB	Output	Reference Circuit 1
8	8	VS+	Supply	

**Applications Information**

**Product Description**

The EL2227 is a dual voltage feedback operational amplifier designed especially for DMT ADSL and other applications requiring very low voltage and current noise. It also features low distortion while drawing moderately low supply current and is built on Elantec's proprietary high-speed complementary bipolar process. The EL2227 use a classical voltage-feedback topology which allows them to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2227 allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators.

**ADSL CPE Applications**

The low noise EL2227 amplifier is specifically designed for the dual differential receiver amplifier function with ADSL transceiver hybrids as well as other low-noise amplifier applications. A typical ADSL CPE line interface circuit is shown in Figure 38. The EL2227 is used in receiving DMT down stream signal. With careful transceiver hybrid design and the EL2227 1.9nV/√Hz voltage noise and 1.2pA/√Hz current noise performance, -140dBm/Hz system background noise performance can be easily achieved.

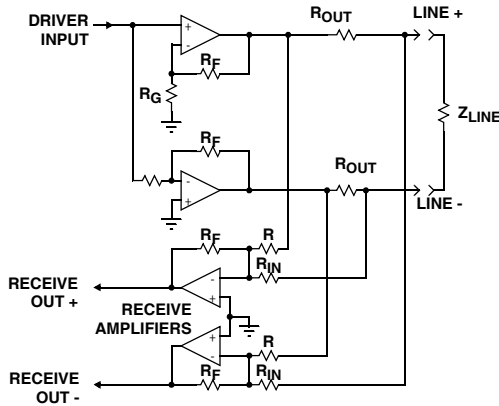


FIGURE 38. TYPICAL LINE INTERFACE CONNECTION

**Disable Function**

The EL2227 is in the standard dual amplifier package without the enable/disable function. A simple way to implement the enable/disable function is depicted below. When disabled, both the positive and negative supply voltages are disconnected (see Figure 39)

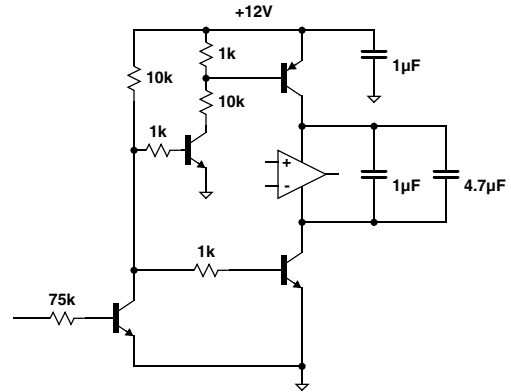


FIGURE 39.

**Power Dissipation**

With the wide power supply range and large output drive capability of the EL2227, it is possible to exceed the +150°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature ( $T_{JMAX}$ ) for all applications to determine if power supply voltages, load conditions, or package type need to be modified for the EL2227 to remain in the safe operating area. These parameters are related as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} \times PD_{MAXTOTAL}) \quad (EQ. 1)$$

where:

$PD_{MAXTOTAL}$  is the sum of the maximum power dissipation of each amplifier in the package ( $PD_{MAX}$ )

$PD_{MAX}$  for each amplifier can be calculated as follows:

$$PD_{MAX} = 2 \times V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad (EQ. 2)$$

where:

$T_{MAX}$  = Maximum Ambient Temperature

$\theta_{JA}$  = Thermal Resistance of the Package

$PD_{MAX}$  = Maximum Power Dissipation of 1 Amplifier

$V_S$  = Supply Voltage

$I_{SMAX}$  = Maximum Supply Current of 1 Amplifier

$V_{OUTMAX}$  = Maximum Output Voltage Swing of the Application

$R_L$  = Load Resistance

To serve as a guide for the user, we can calculate maximum allowable supply voltages for the example of the video cable-driver below since we know that  $T_{JMAX} = +150^\circ\text{C}$ ,  $T_{MAX} = +75^\circ\text{C}$ ,  $I_{SMAX} = 9.5\text{mA}$ , and the package  $\theta_{JA}$ s are shown in Table 1. If we assume (for this example) that we are driving a back-terminated video cable, then the

maximum average value (over duty-cycle) of  $V_{OUTMAX}$  is 1.4V, and  $R_L = 150\Omega$ , giving the results seen in Table 1.

TABLE 1.

PART	PACKAGE	$\theta_{JA}$	MAX $PD_{ISS}$ @ $T_{MAX}$	MAX $V_S$
EL2227CS	SO8	160°C/W	0.406W @ +85°C	
EL2227CY	MSOP8	206°C/W	0.315W @ +85°C	

### Single-Supply Operation

The EL2227 have been designed to have a wide input and output voltage range. This design also makes the EL2227 an excellent choice for single-supply operation. Using a single positive supply, the lower input voltage range is within 200mV of ground ( $R_L = 500\Omega$ ), and the lower output voltage range is within 875mV of ground. Upper input voltage range reaches 3.6V, and output voltage range reaches 3.8V with a 5V supply and  $R_L = 500\Omega$ . This results in a 2.625V output swing on a single 5V supply. This wide output voltage range also allows single-supply operation with a supply voltage as high as 28V.

### Gain-Bandwidth Product and the -3dB Bandwidth

The EL2227 have a gain-bandwidth product of 137MHz while using only 5mA of supply current per amplifier. For gains greater than 2, their closed-loop -3dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 2, higher-order poles in the amplifiers' transfer function contribute to even higher closed loop bandwidths. For example, the EL2227 have a -3dB bandwidth of 115MHz at a gain of +2, dropping to 28MHz at a gain of +5. It is important to note that the EL2227 have been designed so that this "extra" bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2227 in a gain of +2 only exhibit 0.5dB of peaking with a 1000 $\Omega$  load.

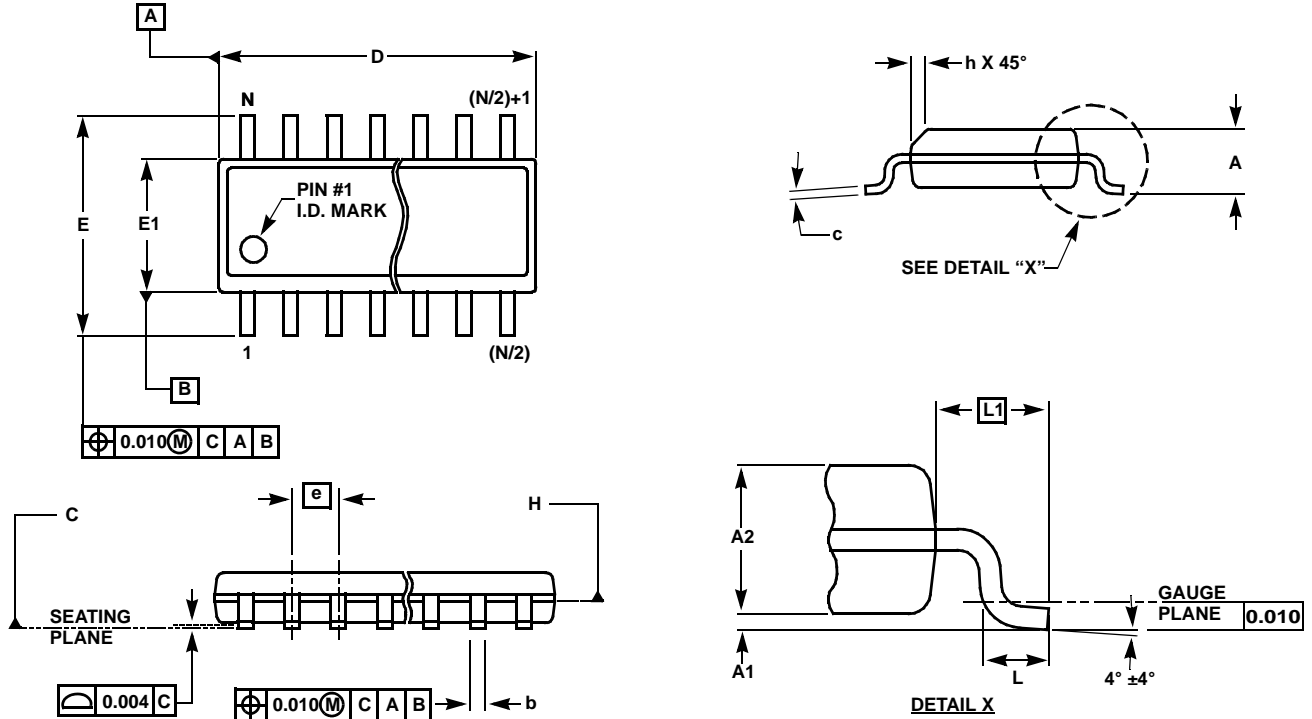
### Output Drive Capability

The EL2227 have been designed to drive low impedance loads. They can easily drive 6V<sub>p-p</sub> into a 500 $\Omega$  load. This high output drive capability makes the EL2227 an ideal choice for RF, IF and video applications.

### Printed-Circuit Layout

The EL2227 are well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1 $\mu$ F ceramic capacitor is recommended for bypassing both supplies. Lead lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5k $\Omega$  because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.

**Small Outline Package Family (SO)**



**MDP0027**

**SMALL OUTLINE PACKAGE FAMILY (SO)**

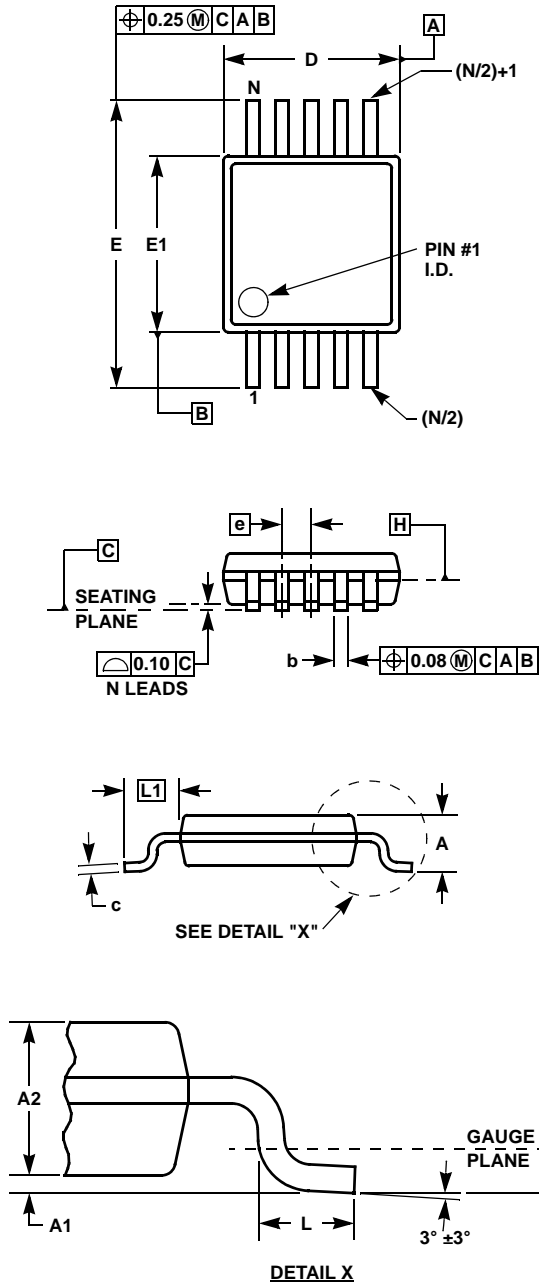
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

**NOTES:**

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Mini SO Package Family (MSOP)



MDP0043  
MINI SO PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	MSOP8	MSOP10		
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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