ENC28J60

ENC28J60 Rev. B7 Silicon Errata

The ENC28J60 (Rev. B7) parts you have received conform functionally to the Device Data Sheet (DS39662**C**), except for the anomalies described below. Any data sheet clarification issues related to this device will be reported in a separate data sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to ENC28J60 devices with the following revision identifier:

Part Number	Device Revision (EREVID)
ENC28J60	0000 0110

EREVID is located at address 0312h in the device's memory register space.

1. Module: Reset

After sending an SPI Reset command, the PHY clock is stopped but the ESTAT.CLKRDY bit is not cleared. Therefore, polling the CLKRDY bit will not work to detect if the PHY is ready.

Additionally, the hardware start-up time of 300 μs may expire before the device is ready to operate.

Work around

After issuing the Reset command, wait for at least 1 ms in firmware for the device to be ready.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: Oscillator (CLKOUT Pin)

No output is available on CLKOUT during Power Save mode (ECON2.PWRSV = 0).

Work around

If the host controller uses the CLKOUT signal as the system clock, do not enable Power Save mode.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: Memory (Ethernet Buffer)

The receive hardware maintains an internal Write Pointer that defines the area in the receive buffer where bytes arriving over the Ethernet are written. This internal Write Pointer should be updated with the value stored in ERXST whenever the Receive Buffer Start Pointer, ERXST, or the Receive Buffer End Pointer, ERXND, is written to by the host microcontroller.

Sometimes, when ERXST or ERXND is written to, the exact value, 0000h, is stored in the Internal Receive Write Pointer instead of the ERXST address.

Work around

Use the lower segment of the buffer memory for the receive buffer, starting at address 0000h. For example, use the range (0000h to n) for the receive buffer, and ((n + 1) – 8191) for the transmit buffer.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: Interrupts

The Receive Packet Pending Interrupt Flag (EIR.PKTIF) does not reliably/accurately report the status of pending packets.

Work around

In the Interrupt Service Routine, if it is unknown if a packet is pending and the source of the interrupt is unknown, switch to Bank 1 and check the value in EPKTCNT.

If polling to see if a packet is pending, check the value in EPKTCNT.

Note:	This errata applies only to the interrupt flag. If the receive packet pending interrupt is enabled, the $\overline{\text{INT}}$ pin will continue to reliably become asserted when a packet arrives. The receive packet pending interrupt is cleared in the same manner as described in the data sheet.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: PHY

The automatic polarity detection and correction features of the PHY layer do not work as described. This may cause poor receive network performance, or no receive activity, with some link partners.

Work around

When designing the application, always verify that the TPIN+ and TPIN- pins are connected correctly.

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: PHY

The external resistor value recommended for RBIAS in the current data sheet differs from previous silicon revisions.

Work around

Rev. B7 silicon requires that a 2.32 kΩ, 1% external resistor be attached from the RBIAS pin to ground.

Note:	ENC28J60 silicon revisions B1 and B4 require a 2.70 kΩ, RBIAS resistor. Silicon revisions B5 and B7 require a 2.32 kΩ, RBIAS resistor. Using an incorrect resistor value will cause the Ethernet transmit waveform to violate IEEE 802.3™ specification requirements.

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: PHY

The PHY Half-Duplex Loopback mode, enabled when PHCON1.PDPXMD = 0, PHCON2.HDLDIS = 0, PHCON2.FRCLNK = 1 or a link partner is connected, does not loop packets back to itself reliably.

Work around

Perform loopback diagnostics in full duplex using an external loopback connector/cable. To avoid looping occasional packets back to one self, PHCON2.HDLDIS should be set by the host controller.

PHCON2.HDLDIS is cleared by default.

Date Codes that pertain to this issue:

All engineering and production devices.

8. Module: PHY

The PHY Full-Duplex Loopback mode, enabled when PHCON1.PDPXMD = 1 and PHCON1.PLOOPBK = 1, does not loop packets back to itself reliably.

Work around

Perform loopback diagnostics in full duplex using an external loopback connector/cable.

Date Codes that pertain to this issue:

All engineering and production devices.

9. Module: PHY LEDs

When the PHLCON register is programmed to output the duplex status and collision activity on the same LED (‘1110b’), only the duplex status will be displayed. (For example, the LED will be illuminated when in Full-Duplex mode and extinguished when in Half-Duplex mode, regardless of collision activity.)

Work around

When Half-Duplex mode is being used, program the PHLCON register’s LxCFG bits with ‘0011b’ to display the collision status. When Full-Duplex mode is being used, program the PHLCON register’s LxCFG bits with ‘0101b’ to display the duplex status.

Date Codes that pertain to this issue:

All engineering and production devices.

10. Module: Transmit Logic

In Half-Duplex mode, a hardware transmission abort – caused by excessive collisions, a late collision or excessive deferrals – may stall the internal transmit logic. The next packet transmit initiated by the host controller may never succeed. That is, ECON1.TXRTS could remain set indefinitely.

Work around

Before attempting to transmit a packet (setting ECON1.TXRTS), reset the internal transmit logic by setting ECON1.TXRST and then clearing ECON1.TXRST. The host controller may wish to issue this Reset before any packet is transmitted (for simplicity), or it may wish to conditionally reset the internal transmit logic based on the Transmit Error Interrupt Flag (EIR.TXERIF), which will become set whenever a transmit abort occurs.

Clearing ECON1.TXRST may cause a new transmit error interrupt event (with EIR.TXERIF becoming set). Therefore, the interrupt flag should be cleared after the Reset is completed.

Date Codes that pertain to this issue:

All engineering and production devices.

11. Module: Memory (Ethernet Buffer)

The receive hardware may corrupt the circular receive buffer (including the Next Packet Pointer and receive status vector fields) when an even value is programmed into the ERXRDPTH:ERXRDPTL registers.

Work around

Ensure that only odd addresses are written to the ERXRDPT registers. Assuming that ERXND contains an odd value, many applications can derive a suitable value to write to ERXRDPT by subtracting one from the Next Packet Pointer (a value always ensured to be even because of hardware padding) and then compensating for a potential ERXST to ERXND wraparound. Assuming that the receive buffer area does not span the 1FFFh to 0000h memory boundary, the logic in Example 1 will ensure that ERXRDPT is programmed with an odd value:

EXAMPLE 1:

```
if (Next Packet Pointer – 1 < ERXST) or
(Next Packet Pointer – 1 > ERXND)
    then:
ERXRDPT = ERXND
    else:
ERXRDPT = Next Packet Pointer – 1
```

Date Codes that pertain to this issue:

All engineering and production devices.

12. Module: Transmit Logic

If a collision occurs after 64 bytes have been transmitted, the transmit logic may not set the Late Collision Error bit (ESTAT.LATECOL).

Work around

Whenever a late collision potentially can occur (both EIR.TXERIF and ESTAT.TXABRT bits will be set), read the transmit status vector and check the transmit late collision bit (bit 29).

Date Codes that pertain to this issue:

All engineering and production devices.

13. Module: PHY

When transmitting in Half-Duplex mode with some link partners, the PHY will sometimes incorrectly interpret a received link pulse as a collision event. If less than, or equal to, MACLCON2 bytes have been transmitted when the false collision occurs, the MAC will abort the current transmission, wait a random back-off delay and then automatically attempt to retransmit the packet from the beginning – as it would for a genuine collision.

If greater than MACLCON2 bytes have been transmitted when the false collision occurs, the event will be considered a late collision by the MAC and the packet will be aborted without retrying. This causes the packet to not be delivered to the remote node. In some cases, the abort will fail to reset the transmit state machine.

Work around

Implement a software retransmit mechanism whenever a late collision occurs.

When a late collision occurs, the associated bit in the transmit status vector will be set. Also, the EIR.TXERIF bit will become set, and if enabled, the transmit error interrupt will occur.

If the transmit state machine does not get reset, the ECON1.TXRTS bit will remain set and no transmit interrupt will occur (the EIR.TXIF bit will remain clear).

As a result, software should detect the completion of a transmit attempt by checking both TXIF and TXERIF. If the Transmit Interrupt (TXIF) did not occur, software must clear the ECON1.TXRTS bit to force the transmit state machine into the correct state. The logic in Example 2 will accomplish a transmission and any necessary retransmissions with a maximum retry abort.

Date Codes that pertain to this issue:

All engineering and production devices.

EXAMPLE 2:

```
ECON1.TXRST  = 1
ECON1.TXRST  = 0
EIR.TXERIF   = 0
EIR.TXIF     = 0
ECON1.TXRTS  = 1
while(EIR.TXIF = 0 and EIR.TXERIF = 0)
      NOP
ECON1.TXRTS  = 0
read tsv
for retrycount = 0 to 15
   if (EIR.TXERIF and tsv<Transmit Late Collision>) then
      ECON1.TXRST  = 1
      ECON1.TXRST  = 0
      EIR.TXERIF   = 0
      EIR.TXIF     = 0
      ECON1.TXRTS  = 1
      while(EIR.TXIF = 0 and EIR.TXERIF = 0)
            NOP
      ECON1.TXRTS  = 0
      read tsv
   else
      exit for
   end if
next retrycount
```

14. Module: PHY

With some LEDs, the LED auto-polarity detection circuit misdetects the connected polarity of the LED upon Reset. As a result, the LED output pin will sink current when it should be sourcing current and vice versa.

The LED will visually appear inverted. For example, an LED configured to display the link status will be illuminated when no link is present and extinguished when a link has been established.

The likelihood of a misdetection will vary with temperature. If LEDB is misdetected, the PHCON1.PDPXMD bit will also reset to the incorrect state.

Work around

Place a resistor in parallel with the LED. The resistor value needed is not critical. Resistors between 1 kΩ and 100 kΩ are recommended.

Date Codes that pertain to this issue:

All engineering and production devices.

15. Module: DMA

If the DMA module is operated in Checksum mode (ECON1.CSUMEN, DMAST = 1) at any time while a packet is currently being received from the Ethernet (ESTAT.RXBUSY = 1), the packet being received will be aborted.

The packet abort will cause the Receive Error Interrupt Flag (EIR.RXERIF) to be set, the interrupt will occur (if enabled) and the Buffer Error Status bit (ESTAT.BUFER) also will become set.

The packet will be permanently lost.

Work around

Do not use the DMA module to perform checksum calculations. Instead, perform checksums in software.

This problem does not affect the DMA copy operation (ECON1.CSUMEN = 0).

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (10/2007)

Original revision. Silicon errata issues 1 (Reset), 2 (Oscillator – CLKOUT Pin), 3 (Memory – Ethernet Buffer), 4 (Interrupts), 5-8 (PHY), 9 (PHY LEDs), 10 (Transmit Logic), 11 (Memory – Ethernet Buffer), 12 (Transmit Logic), 13-14 (PHY) and 15 (DMA).

Rev B Document (07/2008)

Updated the revision of the referenced data sheet. Changed the revision identifier for this device as the previous version contained an error.

NOTES:

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