CS1500

Digital Power Factor Correction IC

Features

- Digital EMI Noise Shaping
- Excellent Efficiency Under All Load Conditions
- Minimal External Devices Required
- Optimized Digital Loop Compensation
- Comprehensive Safety Features
  - Undervoltage Lockout (UVLO)
  - Output Overvoltage Protection
  - Input Current Limiting
  - Output Overpower Protection
  - Input Brownout Protection
  - Open/short Loop Protection for IAC & FB Pins
  - Thermal Shutdown

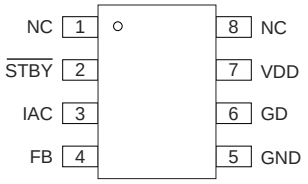
Description

The CS1500 is a high-performance power factor correction (PFC) controller for universal AC input, which uses a proprietary digital algorithm for discontinuous conduction mode (DCM) with variable on-time and variable frequency control, ensuring unity power factor.

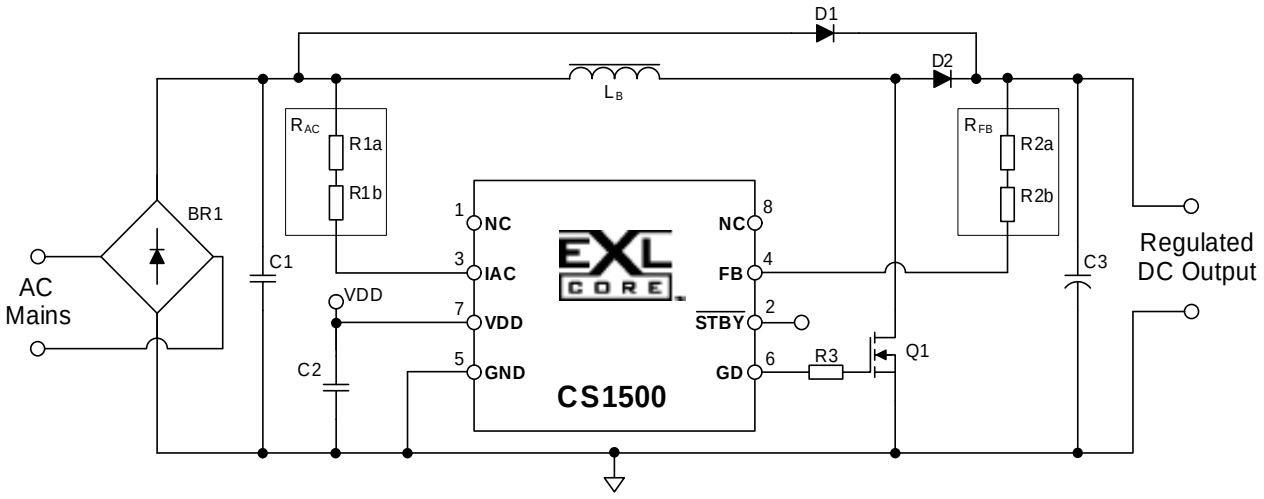
The CS1500 incorporates all the safety features necessary for robust and compact PFC stages. In addition, it has burst mode control to lower the light-load/standby losses to a minimum. Protection features such as overvoltage, overcurrent, overpower, open- and short-circuit protection, overtemperature, and brownout help protect the device during abnormal transient conditions.

The digital controller optimizes the system stability and transient performance, simplifies the PFC design, reduces the external component count and BOM costs. The simple design and minimum cost makes CS1500 the ideal choice for PFC up to 300 watts.

Pin Assignments



8-lead SOIC



Advance Product Information

This document contains information for a product under development. Cirrus Logic reserves the right to modify this product without notice.

Table 1. Pin Descriptions

Pin Name	Pin #	I/O	Description
NC	1, 8	-	**NC** — No connections
$\overline{\text{STBY}}$	2	IN	**Remote On/Off Control** — A voltage below 0.8 V shuts down the IC (not latched) and brings the device into low power consumption mode. The input has an internal 600 kΩ pull-up resistor to the VDD pin and should be driven with an open-collector device.
IAC	3	IN	**Rectifier Voltage Sense** — A current proportional to the rectified line voltage (V_{rect}) is fed into this pin. The current is measured with an A/D converter.
FB	4	IN	**Link Voltage Sense** — A current proportional to the output link voltage (V_{link}) of the PFC is fed into this pin. The current is measured with an A/D converter.
GND	5	-	**Ground** — Current return for both the input signal portion of the IC and the gate driver.
GD	6	OUT	**Gate Driver Output** — The totem pole stage is able to drive the power MOSFET with a peak current of 0.5 A source and 1.0 A sink. The high-level voltage of this pin is clamped at V_Z to avoid excessive gate voltages.
VDD	7	IN	**IC Supply Voltage** — Supply voltage of both the input signal portion of the IC and the gate driver.

1. CHARACTERISTICS AND SPECIFICATIONS

1.1 Absolute Maximum Ratings

Pin	Symbol	Parameter	Value	Unit
7	V_{DD}	IC Supply Voltage	V_Z	V
1,2,3,4,8	-	Analog Input Maximum Voltage	-0.5 to V_Z	V
3,4	-	Analog Input Maximum Current	50	mA
6	V_{GD}	Gate Drive Output Voltage	-0.3 to V_Z	V
6	I_{GD}	Gate Drive Output Current	-1.0 / +0.5	A
-	P_D	Total Power Dissipation @ T_A=50° C	600	mW
	T_A	Operating Ambient Temperature Range[1]	-40 to +125	ºC
-	T_J	Junction Temperature Operating Range	-40 to +125	ºC
-	T_{Stg}	Storage Temperature Range	-65 to +150	ºC

1.2 Electrical Characteristics

(T_A = 25º C, V_{DD} = 13V, -40º < T_J < +125º C, C_L=1nF between pin GD and GND, all voltages are measured with respect to GND; all current are positive when flowing into the IC; unless otherwise specified). Recommended V_{DD} = 10 – 15 V.

Parameter	Condition	Symbol	Min	Typ	Max	Unit
VDD Supply Voltage						
Turn-on Threshold Voltage	V_{DD} Increasing	$V_{DD(on)}$	8.4	8.8	9.3	V
Turn-off Threshold Voltage (UVLO)	V_{DD} Decreasing	$V_{DD(off)}$	7.1	7.4	7.9	V
UVLO Hysteresis		V_{Hys}	-	1.3	-	V
Zener Voltage	I_{DD} = 20 mA	V_Z	16.8	17.9	18.5	V
VDD Supply Current						
Start-up Supply Current	V_{DD} = $V_{DD(on)}$	I_{ST}	-	68	80	µA
Standby Supply Current	$\overline{STBY}$ < 0.8 V	I_{SB}	-	80	112	µA
Operating Supply Current	C_L=1nF, $f_{SW(max)}$=70kHz	I_{DD}	-	1.7	1.9	mA
PFC Gate Drive						
Maximum Operating Frequency[6]	V_{DD} = 13V	$f_{SW(max)}$	62	66	70	kHz
Minimum Operating Frequency[6]	V_{DD} = 13V	$f_{SW(min)}$	20	22	23	kHz
Maximum Duty Cycle[6]	V_{DD} = 13V	D_{max}	64	66	68	%
Output Source Resistance	I_{GD} = 100mA,V_{DD} = 13V	R_{OH}	-	9	-	Ω
Output Sink Resistance	I_{GD} = -200mA,V_{DD} = 13V	R_{OL}	-	6	-	Ω
Rising Time	C_L=1nF,V_{DD} = 13V	t_r	-	32	60	ns
Falling Time	C_L=1nF,V_{DD} = 13V	t_f	-	15	30	ns
Output Voltage Low State	I_{GD} = -200mA,V_{DD} = 13V	Vol	-	0.9	1.3	V
Output Voltage High State	I_{GD} = 100mA,V_{DD} = 13V	Voh	11.3	11.8	-	V

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Feedback & Protection [2,3]						
Reference Current [1]	25º C	I_{REF}	-	129	-	µA
Output Voltage at Startup Mode	25º C, 115 VAC	$V_{O(startup)}$	-	360	-	V
Output Voltage at Normal Mode		$V_{O(nom)}$	-	400	-	V
Overvoltage Protection Threshold	25º C, 115 VAC	V_{OVP}	415	418	421	V
Overvoltage Protection Hysteresis		$V_{OVP(Hy)}$	-	4	-	V
Overpower Protection Threshold [2,4]	25º C, 115 VAC		-	130	-	%
Overpower Protection Recovery [2,4]	25º C, 115 VAC		-	100	-	%
Input Brownout Protection Threshold	25º C, GDRV turns off	$V_{BP(th)}$	62	65	69	Vrms
Input Brownout Recovery Threshold	25º C, GDRV turns on	V_{BR}	76	80	83	Vrms
Thermal Protection [1]						
Thermal Shutdown Threshold		T_{SD}	130	143	155	ºC
Thermal Shutdown Hysteresis		$T_{SD(Hy)}$	-	9	-	ºC
STBY Input [5]						
Logic Threshold Low			-	-	0.8	V
Logic Threshold High			Vdd-0.8	-	-	V

NOTES:

1. Specifications guaranteed by design & characterization and correlation with statistical process controls.
2. Specification are based upon a PFC system configured for AC input of 90-265 VAC (Sine), 45/65 Hz, V_{link}= 400 V, R_{AC} = 3 x 1.0 MΩ, R_{FB} = 3 x 1.0 MΩ, C3 = 180 µF, L_B = 360 µH, 90 W. For other V_{link} voltages, refer to Section 4 Application Example.
3. Detailed Calculation See Section 4 Application Example.
4. Overpower protection is scaled to rated power.
5. $\overline{\text{STBY}}$ is designed to be driven by an open collector. The input is internally pulled up with a 600 kΩ resistor.
6. Normal operation mode, see Section 3.2.

1.3 Thermal Characteristics

Symbol	Parameter	Value	Unit
$R\theta_{JA}$	Thermal Resistance (Junction to Ambient)[7].	159	ºC / W
$R\theta_{JC}$	Thermal Resistance (Junction to Case)[7].	39	ºC / W

7. The package thermal impedance is calculated in accordance with JESD 51.

2. TYPICAL ELECTRICAL PERFORMANCE

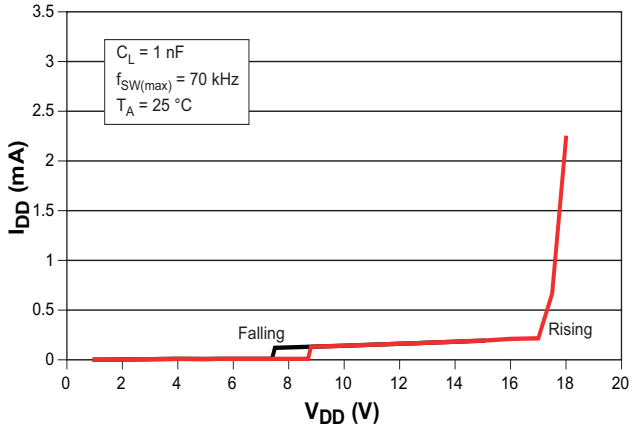


Figure 1. Supply Current vs. Supply Voltage

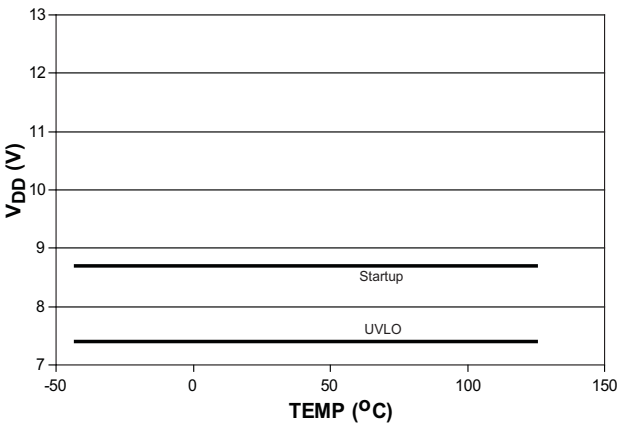


Figure 2. Start-up & UVLO vs. Temp

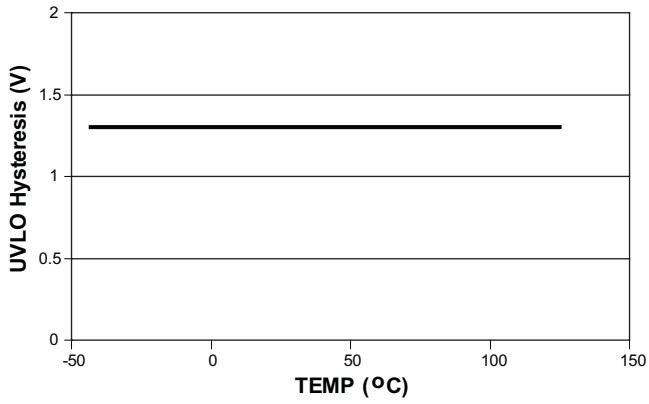


Figure 3. UVLO Hysteresis vs. Temp

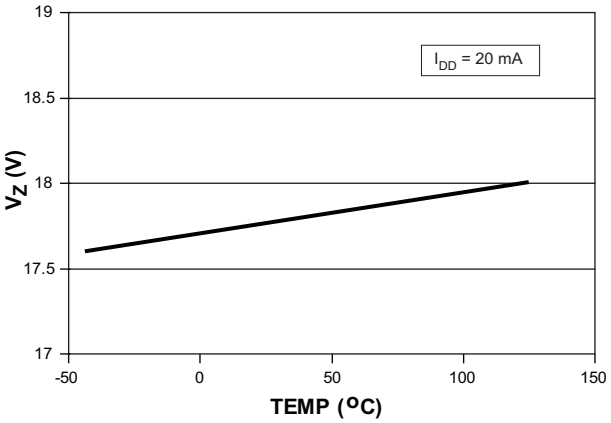


Figure 4. VDD Zener Voltage vs. Temp

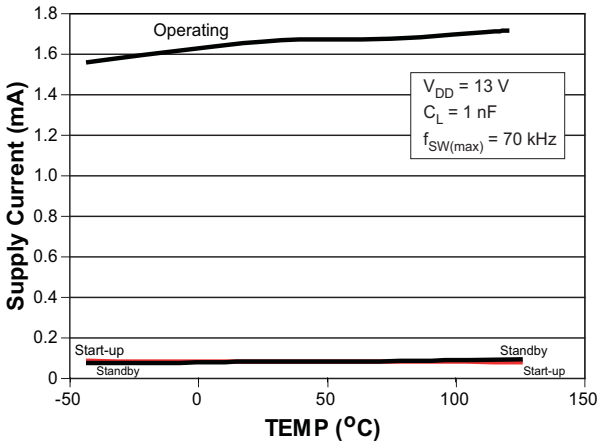


Figure 5. Supply Current (I_{SB}, I_{ST}, I_{DD}) vs. Temp

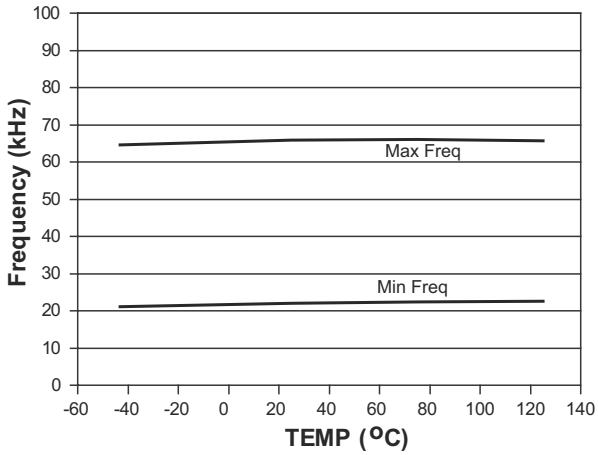


Figure 6. Min/Max Operating Frequency vs. Temp

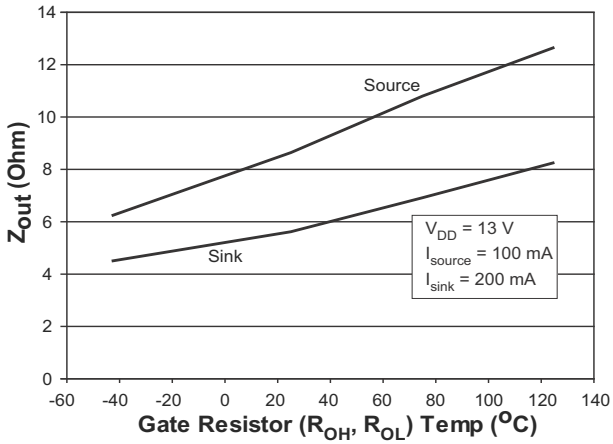


Figure 7. Gate Resistance (R_{OH}, R_{OL}) vs. Temp

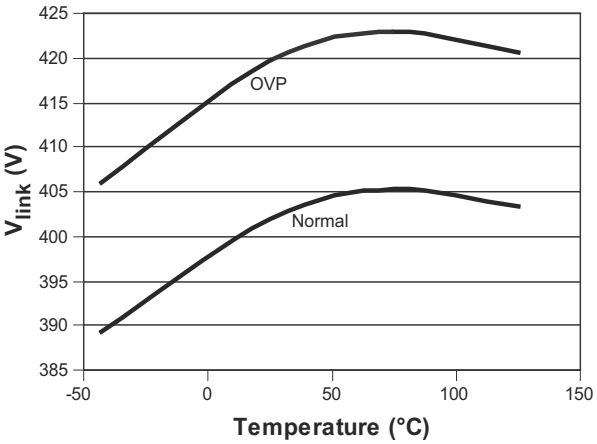


Figure 8. OVP vs. Temp

3. INTRODUCTION

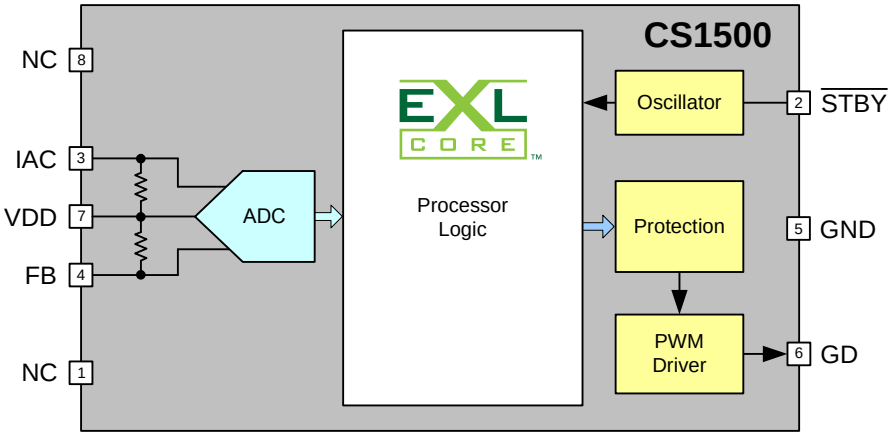


Figure 9. CS1500 Block Diagram

The CS1500 digital power factor controller operates in variable on-time, variable frequency, discontinuous conduction mode (DCM). The CS1500 uses a proprietary digital algorithm to maximize the efficiency and reduce the conductive EMI.

The analog-to-digital converter (ADC) shown in the CS1500 block diagram in Figure 9 is used to sense the PFC output voltage (V_{link}) and the rectified AC line voltage (V_{rect}) by measuring currents through their respective resistors. The magnitudes of these currents are measured as a proportion of a reference current (I_{REF}) that functions as the reference for the ADCs. The digital signal is then processed in a control algorithm which determines the behavior of the CS1500 during start-up, normal operation, and under fault conditions, such as brownout, overvoltage, overcurrent, overpower, and over-temperature conditions.

- **DCM with Variable On-Time, Variable Switching Frequency**

  The CS1500 PFC switching frequency varies with the V_{rect} on a cycle-by-cycle basis, and its digital algorithm calculates the on-time accordingly for unity power factor. Unlike traditional Critical Conduction Mode (CRM) PFC controller, CS1500 operates at its low switching frequency near the zero-crossing point of the AC input voltage, even no switching at all, and it operates at its high switching frequency at the peak of its AC input voltage (this is the opposite of the switching frequency profile for a CRM PFC controller), thus CS1500 reduces switching losses especially under light-load conditions, spreads conducted EMI energy peaks over a wide frequency band and increases overall system efficiency.

- **Optimized Digital Loop Compensation**

  The proprietary digital control engine optimizes the feedback error signal using an adaptive control algorithm, improves system stability and transient response. No external feedback error signal compensation components are required.

- **Overcurrent Mitigation**

  The CS1500s digital controller algorithm limits the ON time of the Power MOSFET by the following equation:

$$T_{on} \leq \frac{0.001126}{V_{rect}}$$

  Where T_{on} is the max time that the power MOSFET is turned on and V_{rect} is the rectified line voltage. In the event of a sudden line surge or sporadic, high dv/dt line voltages, this equation may not limit the ON time appropriately. For this type of line disturbance, additional protection mechanisms such as fusible resistors, fast-blow fuses, or other current-limiting devices are recommended.

- **Over Voltage Protection**

  Under steady-state conditions, the voltage loop keeps PFC output voltage close to its nominal value. Under light load startup or feedback loop open conditions, the output voltage may pass the overvoltage protection threshold. The digital control engine initiates a fast response loop to shut down gate driving signal to reduce the energy delivered to the output for PFC capacitor protection. When the link voltage drop below V_{OVP}-$V_{OVP(Hy)}$, PFC resumes normal operation.

3.1 PFC Operating Frequency

One key feature of the CS1500 is its operating frequency profile. Figure 10 illustrates how the frequency varies over half cycle of the line voltage in steady-state operation. When power is first applied to the CS1500, it first examines the line voltage and adapts its operating frequency to the exposed line voltage as shown in Figure 11. The operating frequency is varied in about a 2-to-1 ratio from the peak to the trough. During start-up the control algorithm limits the maximum on-time, provides nearly square-wave envelop current within every half line cycle by adjusting the operating frequency for fast startup behavior.

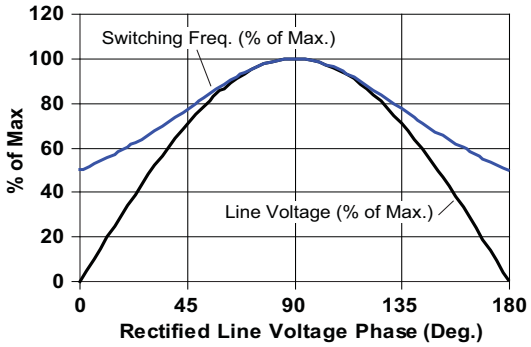


Figure 10. Switching Frequency vs. Phase Angle

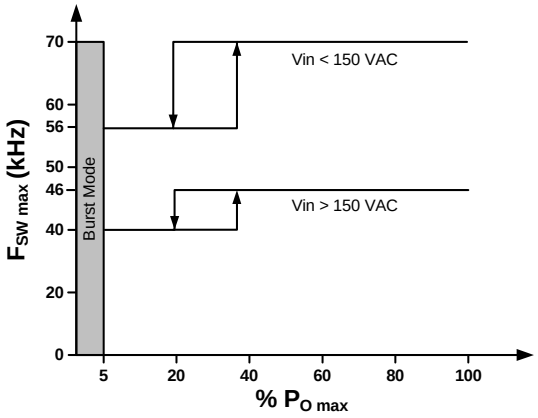


Figure 11. Switching Frequency vs. Output Power

Figure 11 illustrates how the operating frequency (as a percentage of maximum frequency) changes with output power and the peak of the line voltage. Burst mode (when P_o below 5%) will be discussed in a later section.

The CS1500 is designed to function as a DCM (discontinuous conduction mode) controller, however it may operate in a quasi-CRM operation mode near the peak periods. For 90~265VAC main input applications, PFC can be also designed in quasi-CRM at a peak of 90VAC and full load as shown in Figure 12.

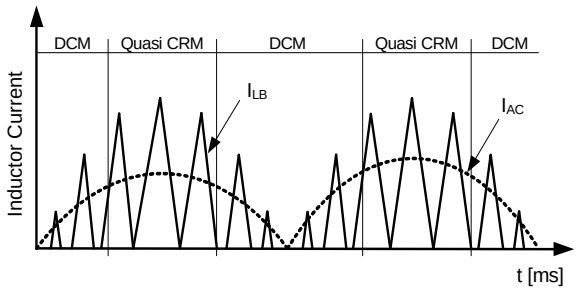


Figure 12. DCM and quasi-CRM Operation with CS1500

3.2 Start-up vs. Normal Operation Mode

CS1500 has two discrete operation modes: Start-up and Normal. Start-up mode will be activated when V_{link} is less than 90% of nominal value and remains active until V_{link} reaches 100% of nominal value, as shown in Figure 13. Startup mode is activated during initial system power-up. Any V_{link} drop to less than 90% of nominal value, such as load change, can cause the system to enter Start-up Mode until V_{link} is brought back into regulation.

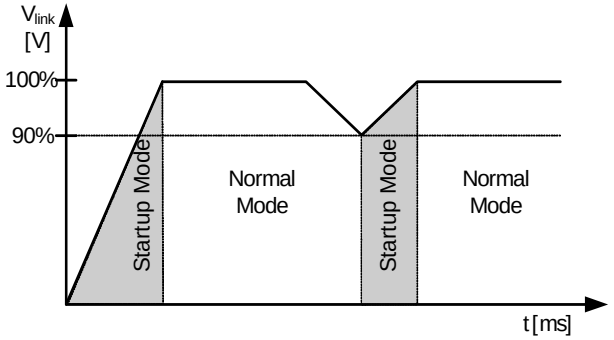


Figure 13. Start-up and Normal Modes

3.3 Burst Mode

Burst mode is utilized to improve system efficiency when the system output power (P_o) is < 5% of nominal. Burst mode is implemented by intermittently disabling the PFC over a full half-line period cycle under light load conditions, as shown in Figure 14.

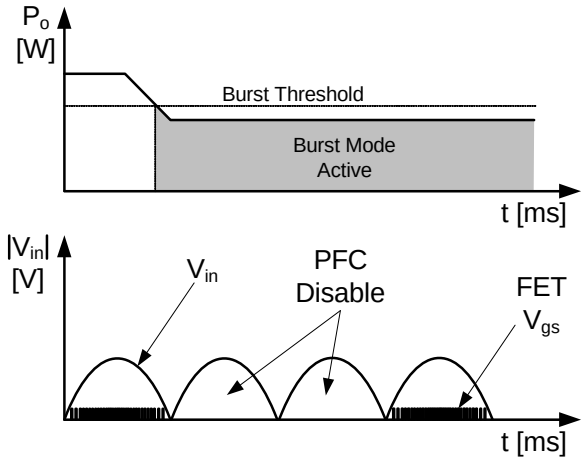


Figure 14. Burst Modes

3.4 Output Power and PFC Boost Inductor

Maximum output power in normal mode is defined by the following equation:

$$P_o = \alpha \times \eta \times (V_{in(min)})^2 \times \frac{V_{link} - (V_{in(min)} \times \sqrt{2})}{2 \times f_{max} \times L_B \times V_{link}} \quad [Eq.1]$$

where, $V_{in(min)}$, V_{link}, and L_B are user defined based on application requirements and maximum operating switching frequency f_{max} = 70kHz. α is a margin factor to guarantee rated power (P_o) against tolerances and transients. α is typically set to 0.9.

The PFC Boost Inductor (LB in Figure 21) value can be calculated using Equation 1 as follows:

$$L_B = \alpha \times \eta \times (V_{in(min)})^2 \times \frac{V_{link} - (V_{in(min)} \times \sqrt{2})}{2 \times f_{max} \times P_o \times V_{link}} \quad [Eq.2]$$

where $V_{in(min)}$ is volts RMS, V_{link} is volts DC, and α is set to 0.9.

3.5 PFC Output Capacitor

The value of the PFC output capacitor should be chosen based upon voltage ripple and hold-up requirements. This is described in more detail in the application section 4.1.6 *PFC Output Capacitor* on page 13. To ensure system stability with the digital controller, the recommended value of the capacitor is within the range of 0.5 µF / watt to 2.0 µF / watt.

3.6 Output Feedback & Regulation

A current proportional to the PFC output voltage, V_{link}, is supplied to the IC on pin FB and is used as a feedback control signal. This current is compared against a fixed-value internal reference current, I_{ref}.

Resistor R_{FB} (shown as R2a & R2b in Figure 21) sets the feedback current and is calculated as follows:

$$R_{FB} = \frac{V_{link} - V_{dd}}{I_{ref}} \quad [Eq.3]$$

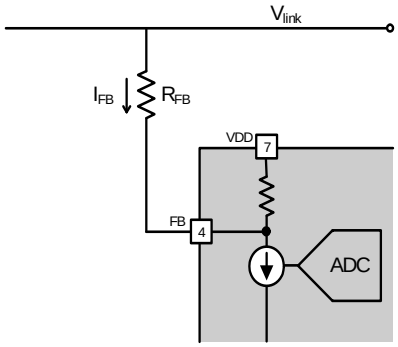


Figure 15. Feedback Input Pin Model

The ADC is used to measure the magnitude of the I_{FB} current through resistor R_{FB}. The magnitude of the I_{FB} current is then compared to an internal reference current, I_{ref}.

By using digital loop compensation, the voltage feedback signal does not require an external compensation network.

It is recommended that a ceramic capacitor of up to 2.2 nF be placed between the FB pin and the VDD pin to filter noise in the layout.

3.7 IAC Signal

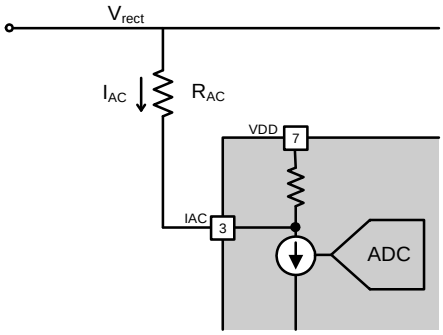


Figure 16. IAC Input Pin Model

A current proportional to the AC input voltage is supplied to the IC on pin IAC and is used by the PFC control algorithm.

Resistor R_{AC} (shown as R1a & R1b in Figure 21) sets the IAC current and is calculated as follows:

$$R_{AC} = R_{FB} \quad [Eq.4]$$

For optimal performance, resistor R_{AC}, R_{FB} should use less than 1% tolerance resistor. Resistors can be separated in two

or more series elements if voltage breakdown or regulatory compliance is of concern.

It is recommended that a ceramic capacitor of up to 2.2 nF be placed between the IAC pin and the VDD pin to filter noise in the layout.

3.8 Brownout Protection

Figure 17 illustrates the brownout protection mechanism whereby the CS1500 enters standby, and upon recovery from brownout, enters normal operation mode. In order to avoid the fault trigger, a digital filter is added for line voltage detection. The measured peak of the line voltage will be clamped to a threshold (128 V) set by the IC within half of a line cycle if it is higher than the threshold. It then decreases the voltage with a slew rate of 5 V / trough (8 ms). The CS1500 initiates a timer when the measured voltage falls below the lower brownout threshold. The IC asserts the brownout protection and stops the gate drive only if the timer reaches more than 56 ms, which is set by the algorithm based on minimum line frequency.

During the brownout state, the device continues monitoring the input line voltage. The device exits the brownout state when the input voltage peak value exceeds the brownout upper threshold for at least 56 ms.

The maximum response time of the brownout protection normally happens at light load conditions. It can be calculated by the following equation:

$$T_{Brownout} = 8\,ms + \frac{8\,ms}{5\,V}(128\,V - V_{BP(th)}) + 56\,ms \quad [Eq.5]$$

$$= 8 + \frac{8}{5}(128 - 95) + 56$$

$$= 116.8\ ms$$

In the brownout state, the PFC gate driver will restart every 3 seconds, trying to regulate V_{link} to nominal value.

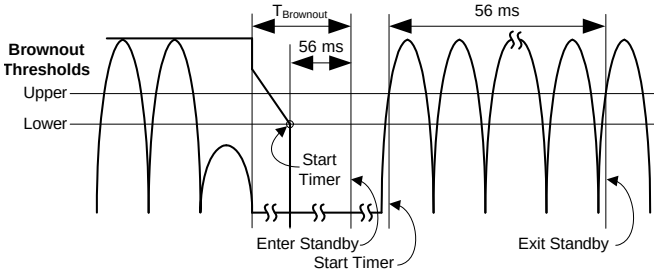


Figure 17. Brownout Sequence

3.9 Overpower Protection

During normal operation, if the load is increased beyond the overpower threshold, the output voltage starts falling. When the output voltage is below the startup threshold voltage, the CS1500 switches to startup mode and the output voltage will rise back again to the nominal value and will operate in normal mode if the load is reduced to a normal level. Otherwise, the PFC oscillates between startup mode and normal mode and the digital engine declares the overpower condition. When the overpower protection is asserted, the IC stops gate drive, goes into a low-power state, and restarts every 3 seconds. In the case of an intermittent or minor fault, the device will continue to regulate the output voltage (V_{link}) to its nominal value.

If the PFC remains in startup mode for longer than a given time, set by the digital controller, it senses an overload condition and initiates the overpower protection.

The CS1500 has the ability to ensure nearly constant overpower constraint over a wide range of line voltages, as shown in Figure 19.

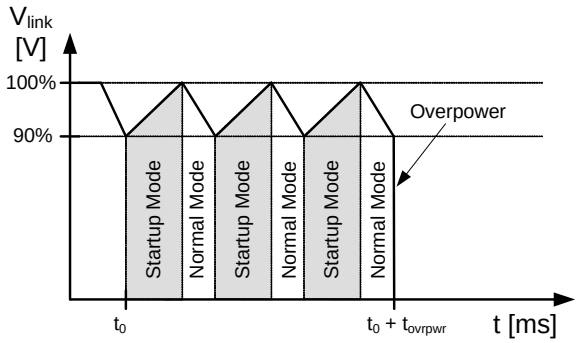


Figure 18. Overpower Protection Mechanism

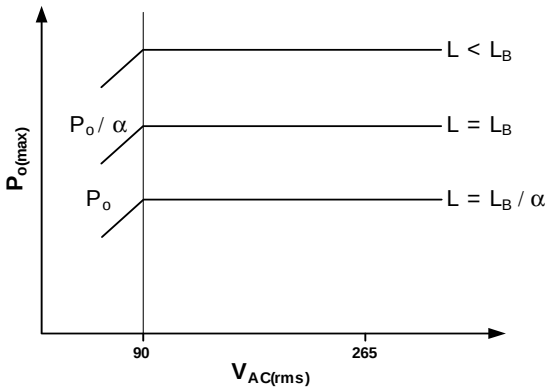


Figure 19. Maximal Output Power vs. Line Voltage

3.10 Overvoltage Protection

The overvoltage protection will trigger immediately and stop the gate drive when the current into the FB pin (I_{OVP}) exceeds 105% of the reference current value (I_{ref}). The IC resumes gate drive switching when the link voltage drops below $V_{OVP} - V_{OVP(HY)}$.

3.11 Open/short Loop Protection

If the PFC output sense resistor R_{FB} fails (open or short to GND), the measured output voltage decreases at a slew rate of about 2V / µs, which is determined by ADC sampling rate. The IC stops the gate drive when the measured output voltage is lower than the measured line voltage. The IC resumes gate drive switching when the current into the FB pin becomes larger than or equal to the current into the IAC pin and V_{link} is

greater than the peak of the line voltage ($V_{rect(pk)}$). The maximum response time of open/short loop protection for R_{FB} is about 150 µs in the CS1500.

If the PFC input sense resistor R_{AC} fails (open or short to GND), the current reference signal supplied to the IC on pin IAC falls to zero. This failure is equivalent to a brownout condition and will be handled by the brownout protection mechanism described in Section 3.8.

3.12 Overcurrent Limiting

Boost inductor saturation is a fatal condition for a PFC converter. To prevent inductor current saturation conditions, the IC utilizes a proprietary digital algorithm that keeps the boost inductor current away from its saturation current. The boost inductor should be designed for full load, minimal line voltage, maximum switching frequency, and with enough margin to prevent saturation in normal operation mode.

3.13 Standby ($\overline{\text{STBY}}$) Function

The standby ($\overline{\text{STBY}}$) pin provides a means by which an external signal can cause the CS1500 to enter into a non-operating, low-power state. The $\overline{\text{STBY}}$ input is intended to be driven by an open-collector/open-drain device. Internal to the pin, there is a pull-up resistor connected to the VDD pin as shown in Figure 20. Since the pull-up resistor has a high impedance, the user may need to provide a filter capacitor (up to 1000 pF) on this pin.

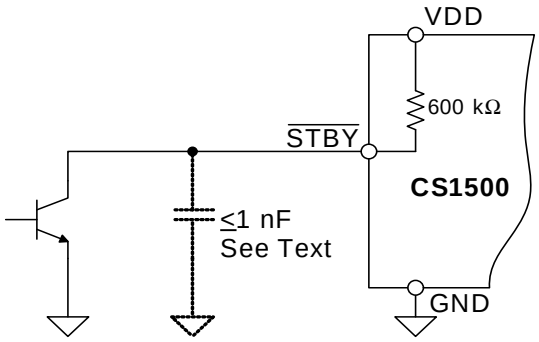


Figure 20. $\overline{\text{STBY}}$ Pin Connection

When the $\overline{\text{STBY}}$ pin is not used, it is recommended that the pin be tied to VDD (pulled high).

4. APPLICATION EXAMPLE

The following sections describe an example application. The example is based upon the typical connection diagram illustrated in Figure 21.

Equations are provided to demonstrate how a user would calculate the values for the components shown in the diagram.

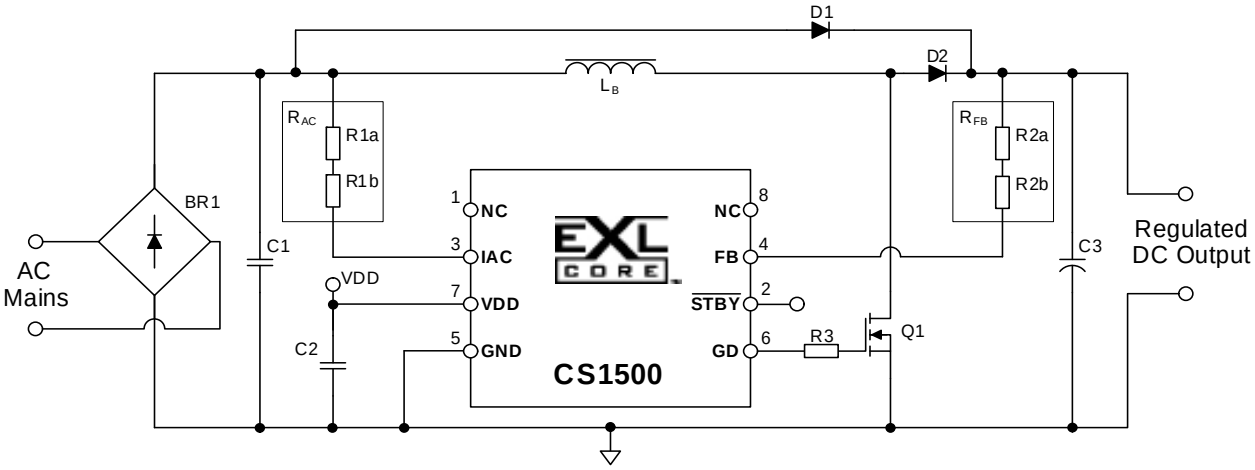


Figure 21. CS1500 Basic Application Circuit

4.1 PFC for Power Supply Application

The following design example is for a universal main input, front-end PFC converter with the following parameters:

$V_{in(min)}$	90 VAC
$V_{in(max)}$	265 VAC
V_{link}	400 V
P_o	90 W

4.1.1 I_{AC} and I_{FB} Sensing Inputs

The rectified AC input voltage (V_{rect}) and boosted PFC output voltage (V_{link}) are sensed as currents into the IC. The sensing currents are set by resistors R_{AC} and R_{FB}, respectively:

$$R_{FB} = \frac{V_{link} - V_{dd}}{I_{ref}} \quad \text{[Eq.6]}$$

$$R_{FB} = \frac{400 - 12}{129 \times 10^{-6}}$$

$$R_{FB} = 3.0\text{M}\Omega$$

$$R_{AC} = R_{FB} \quad \text{[Eq.7]}$$

$$R_{AC} = 3.0\text{M}\Omega$$

Maximum power dissipation in each sense resistor is calculated as follows (the equation ignores the voltage drop across R_{IAC} & R_{IFB}):

$$P(R_{FB}) = \frac{V_{link}^2}{R_{FB}} \quad \text{[Eq.8]}$$

$$P(R_{FB}) = \frac{400^2}{3 \times 10^6}$$

$$P(R_{FB}) = 53.3\text{mW}$$

$$P(R_{AC})max = \frac{[V_{in(max)}]^2}{R_{AC}} \quad \text{[Eq.9]}$$

$$P(R_{AC})max = \frac{265^2}{3 \times 10^6}$$

$$P(R_{AC})max = 23.4\text{mW}$$

4.1.2 PFC Input Filter Capacitor

To achieve unity power factor, a DCM PFC circuit needs an input filtering circuit to bypass the high-frequency current so that the input current consists of the low-frequency portion only. There are two main factors on PFC input filter capacitor selection: its voltage ripple and phase lag, which both will worsen power factor. The filtering capacitance is proportional to P_o and it is suggested as follows:

$$C_1 \geq 3.3\frac{nF}{W} \times P_o \quad \text{[Eq.10]}$$

$$C_1 \geq 3.3 \times 120$$

$$C_1 \geq 390nF = 0.39\mu F$$

Use 0.47 µF for tolerance.

If a PI filter used for suppression of conducted EMI is located on the DC side of the input rectifier, the V_{rect} sense point has to be moved to the second capacitor.

4.1.3 PFC Boost Inductor

The value of the inductor in normal mode can be calculated by the following equation, with $\alpha = 0.9$ as a derating factor to ensure the inductor is sized to guarantee DCM operation and provide a slightly higher power than required by the load:

$$L_B = \alpha \times \eta \times (V_{in(min)})^2 \times \frac{V_{link} - (V_{in(min)} \times \sqrt{2})}{2 \times f_{max} \times P_o \times V_{link}} \quad \text{[Eq.11]}$$

$$L_B = 0.9 \times 0.95 \times 90^2 \times \frac{400 - (90 \times \sqrt{2})}{2 \times (70 \times 10^3) \times 90 \times 400}$$

$$L_B = 374\mu H$$

Choose a 360 µH inductor.

$$I_{LB(pk)} = \frac{4 \times P_o}{\alpha \times \eta \times V_{in(min)} \times \sqrt{2}} \quad \text{[Eq.12]}$$

$$I_{LB(pk)} = \frac{4 \times 90}{0.9 \times 0.95 \times 90 \times \sqrt{2}}$$

$$I_{LB(pk)} = 3.3A$$

η is the efficiency.

The inductor should be designed so that its saturation current meets the following requirement, where 0.001126 is a pre-defined threshold for the current protection algorithm:

$$I_{sat} \leq \frac{0.001126}{L} \quad \text{[Eq.13]}$$

where L is the inductance in Henrys.

4.1.4 PFC MOSFET

In normal mode, the PFC MOSFET peak current is equal to the peak current in the PFC boost inductor:

$$I_{FET(pk)} = I_{LB(pk)} \quad \text{[Eq.14]}$$

$$I_{FET(pk)} = 3.3A$$

4.1.5 PFC Diode

The PFC diode peak current in normal mode is the equal to the inductor peak current:

$$I_{D(pk)} = I_{LB(pk)} \quad \text{[Eq.15]}$$

$$I_{D(pk)} = 3.3A$$

The PFC Diode average current is calculated as follows:

$$I_{D(avg)} = \frac{P_o}{V_{link}} \quad \text{[Eq.16]}$$

$$I_{D(avg)} = \frac{90}{400}$$

$$I_{D(avg)} = 0.225A$$

4.1.6 PFC Output Capacitor

The value of the output capacitor is determined by several requirements. It must meet the voltage ripple and hold-up time requirements and the RMS current in the capacitor should not exceed its RMS current rating.

The following equation defines the size of the output capacitor to meet the output voltage ripple requirements:

$$C_{out(rip)} = \frac{P_O}{2\pi \times f_{line(min)} \times V_{link} \times \Delta V_{link(rip)}} \quad \text{[Eq.17]}$$

$f_{line(min)}$ is the minimum line frequency the design is required to support, V_{link} is the output voltage from the PFC, $\Delta V_{link(rip)}$, is the output voltage ripple requirement in volts peak-to-peak. The equation will provide the value of the output capacitor needed to meet the ripple requirement.

For 10 V of ripple and minimum line frequency of 45 Hz, the equation becomes:

$$C_{out(rip)} = \frac{90}{2\pi \times 45 \times 400 \times 10} = 80\mu F \text{ use } 100\mu F$$

A second requirement that the output capacitor may be required to meet is hold-up time. The value of the capacitor

needed to meet the hold-up time required is defined by the following equation:

$$C_{out(hold)} = \frac{2 \times P_O \times t_{hold}}{\left(V_{link} - \frac{\Delta V_{out(rip)}}{2}\right)^2 - (V_{link(min)})^2} \quad \text{[Eq.18]}$$

t_{HOLD} is the magnitude of the hold-up time in seconds. For 10 ms of hold-up time and $V_{link(min)}$ of 300 V, the equation becomes:

$$C_{out(hold)} = \frac{2 \times 90 \times 0.010}{\left(400 - \frac{10}{2}\right)^2 - (300)^2} = 27\mu F$$

Choose a 100 µF capacitor.

4.1.7 Overvoltage Protection

Overvoltage protection is activated when V_{link} exceeds 105% of the nominal value:

$$V_{ovp} = V_{link} \times 1.05 \quad \text{[Eq.19]}$$

$$V_{ovp} = 400 \times 1.05$$

$$V_{ovp} = 420V$$

While in overvoltage protection mode, gate drive output is disabled. GD output is re-enabled when V_{link} falls below its nominal value.

4.1.8 Summary of Component Values

Designator	Value	Description
R1a	1.5 MΩ	SFR25 axial film res - 0.4W-1%
R1b	1.5 MΩ	SFR25 axial film res - 0.4W-1%
R2a	1.5 MΩ	SFR25 axial film res - 0.4W-1%
R2b	1.5 MΩ	SFR25 axial film res - 0.4W-1%
R3	4.7 Ω	SFR25 axial film res - 0.4W-1%
C1	0.47 µF	ECQ2W474KH
C2	0.47 µF	50V Ceramic cap - X7R
C3	100 µF, 450V	LLS2W101MELA
BR1	4A, 600V	GBU4J-BP
D1	1 A, 600 V	1N4005
D2	1 A, 600 V	STTH1R06
LB	360 µH	Premier Magnetics
Q1	12 A, 500 V	STP12NM50FP
CS1500	PFC Controller	CS1500

5. PERFORMANCE PLOTS

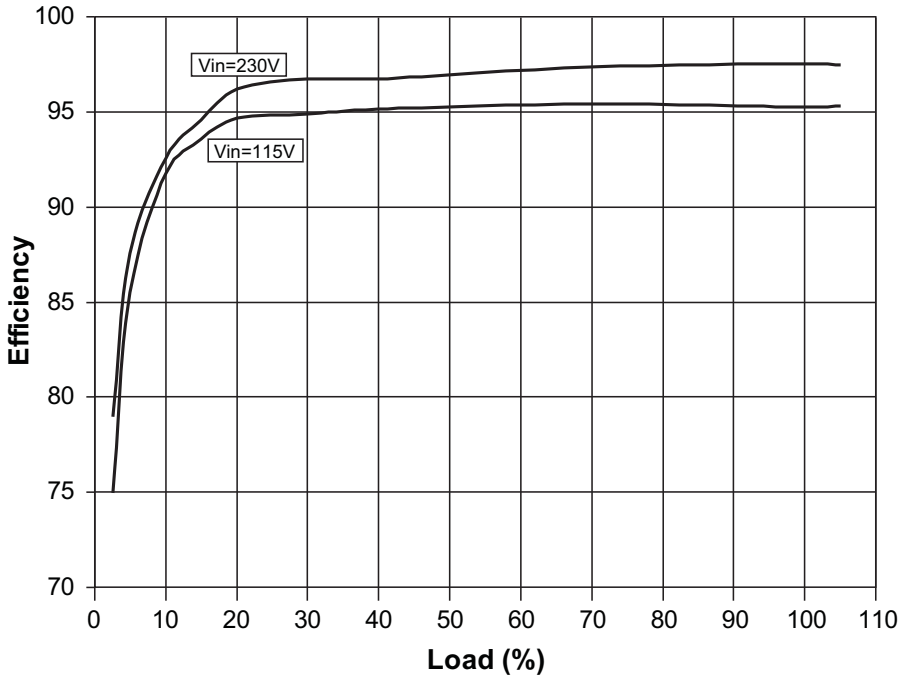


Figure 22. Efficiency vs. Load, Typical

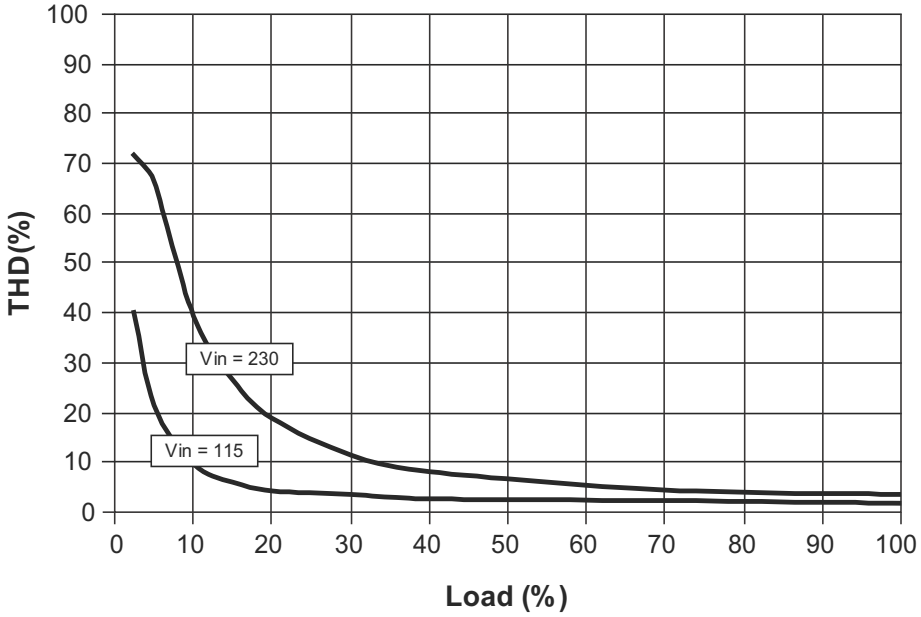


Figure 23. Distortion vs. Load, Typical

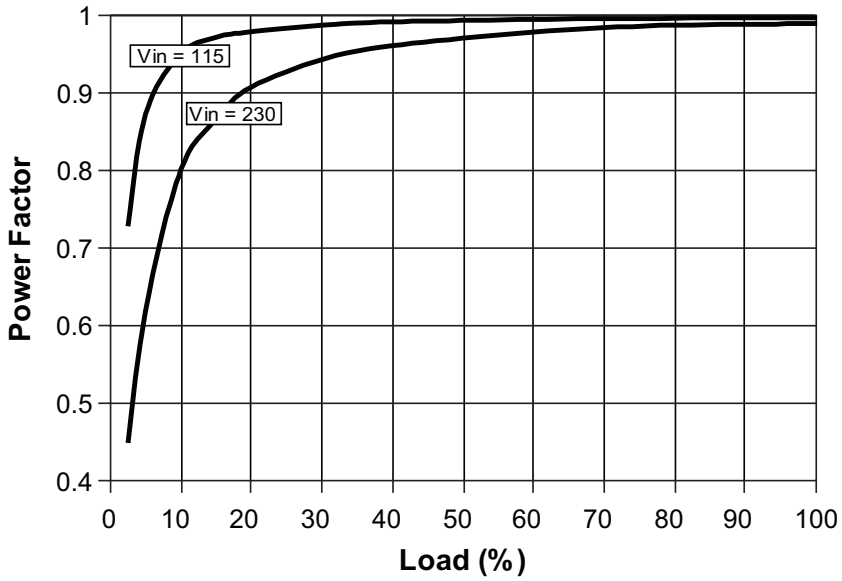


Figure 24. Power Factor vs. Load, Typical

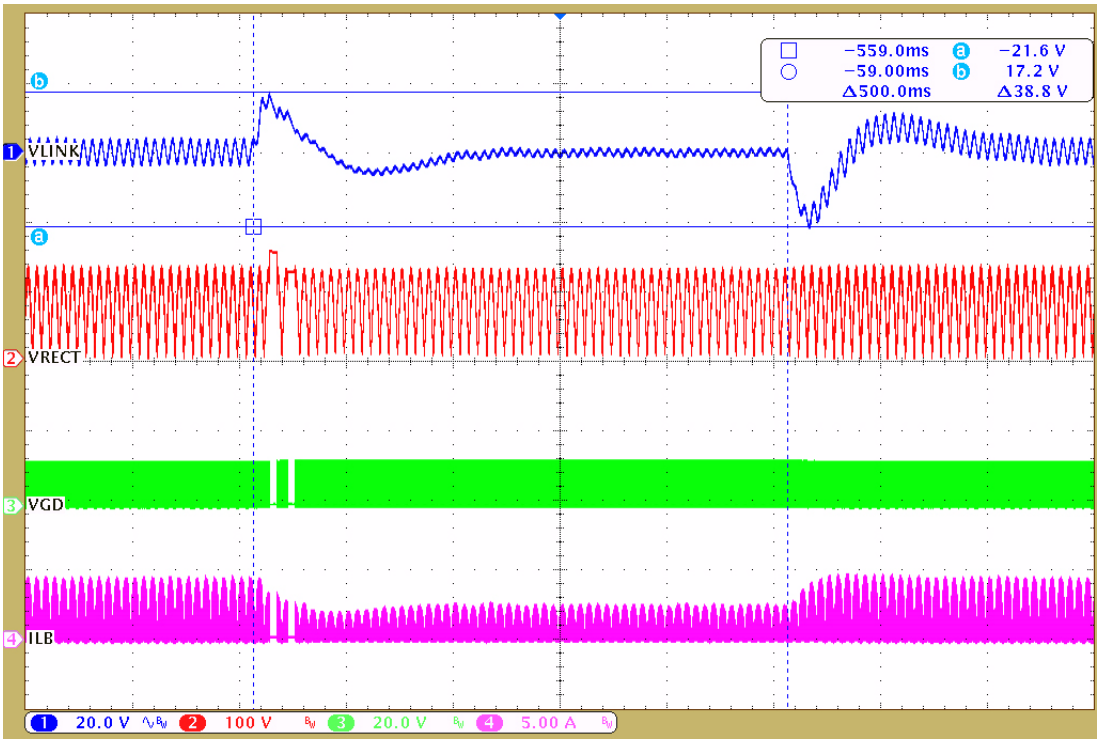


Figure 25. Load Transient — 20% to 80% (60 mA to 240 mA), 0.8 A/µsec Slew, 90 VAC

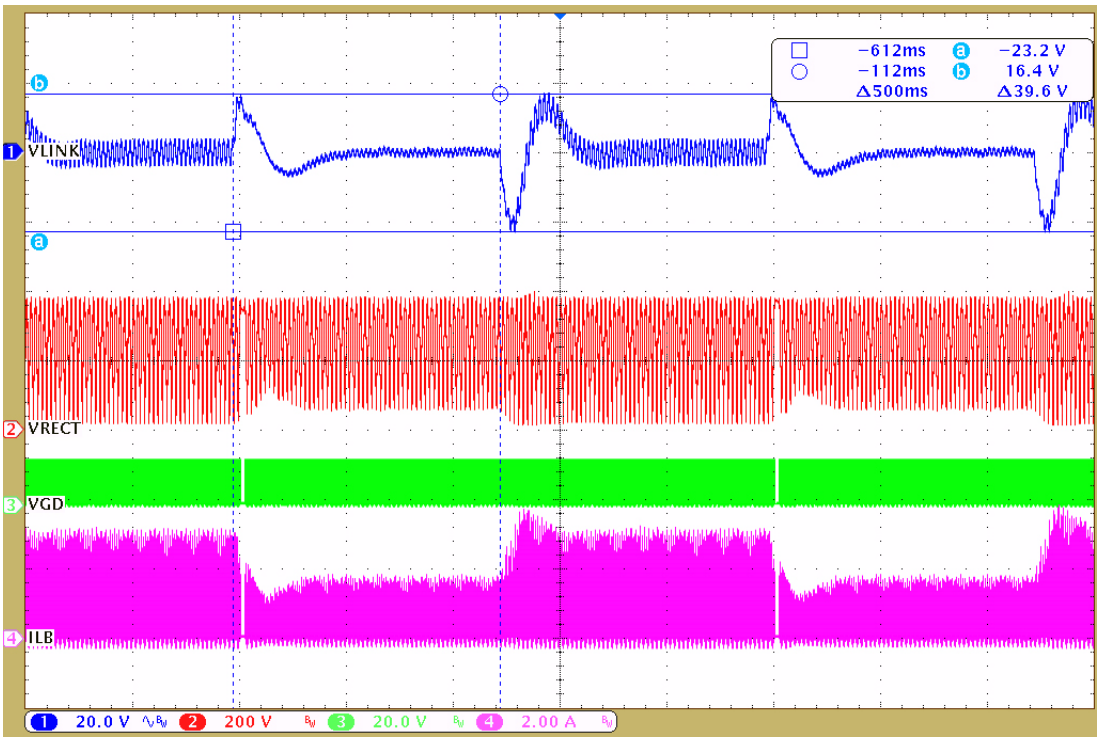


Figure 26. Load Transient — 20% to 80% (60 mA to 240 mA), 0.8 A/µsec Slew, 260 VAC

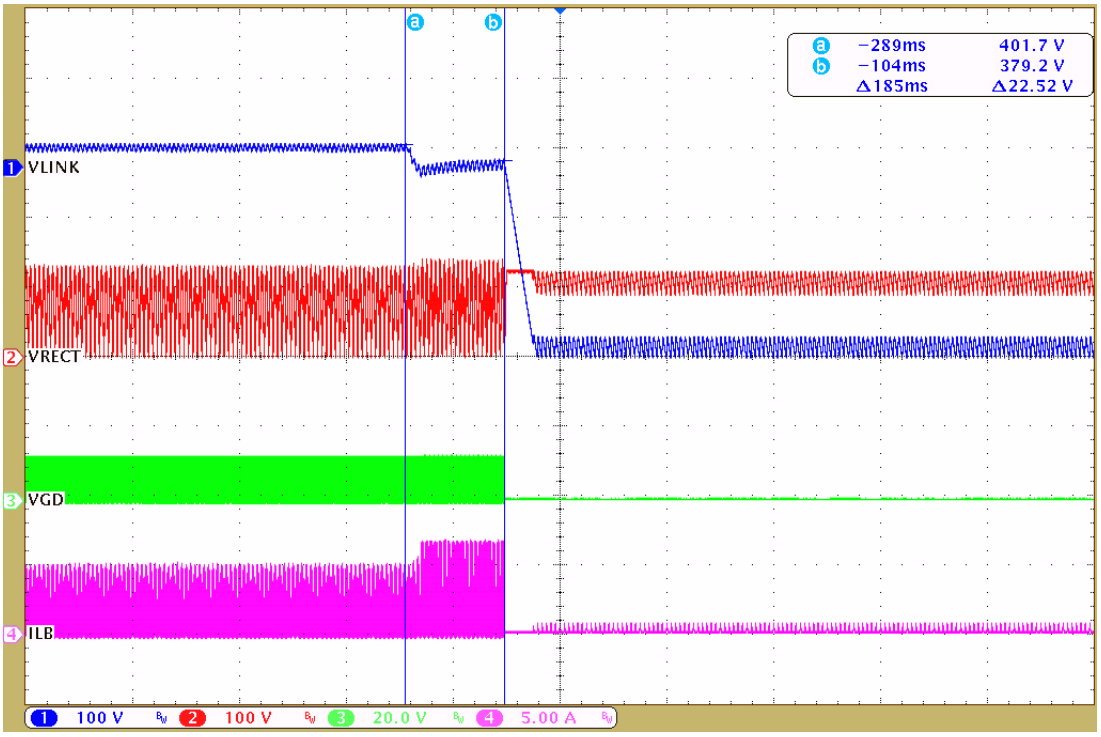


Figure 27. Overload — 240 mA to 500 mA, 90 VAC

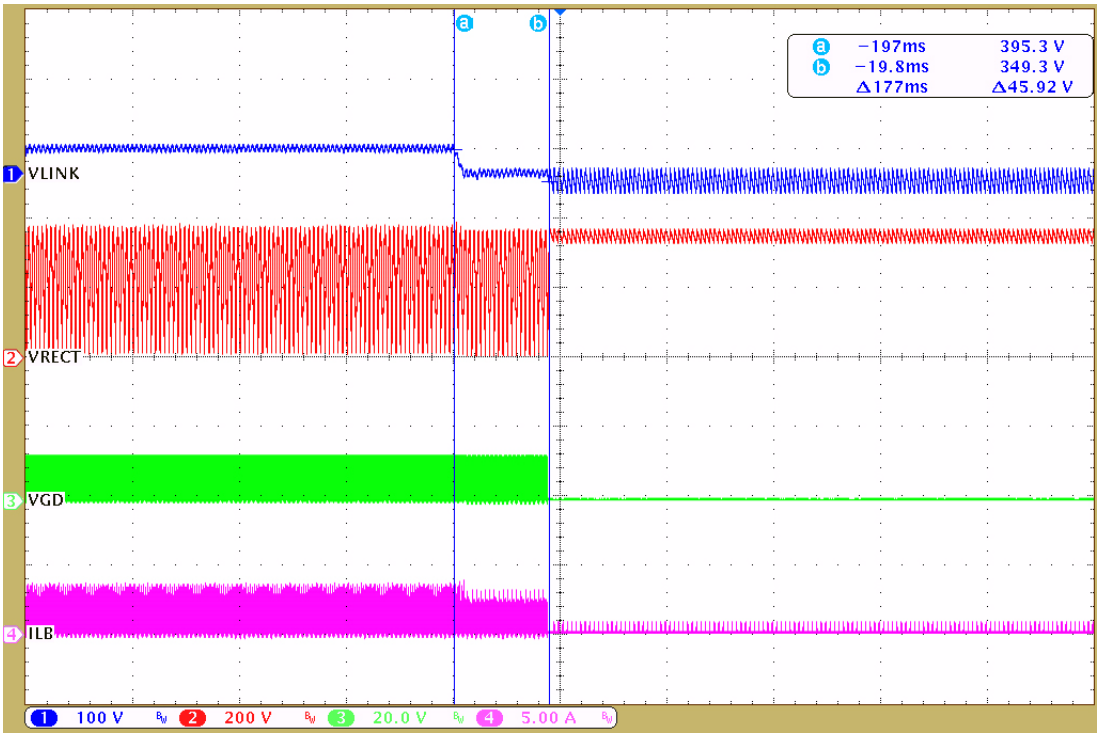


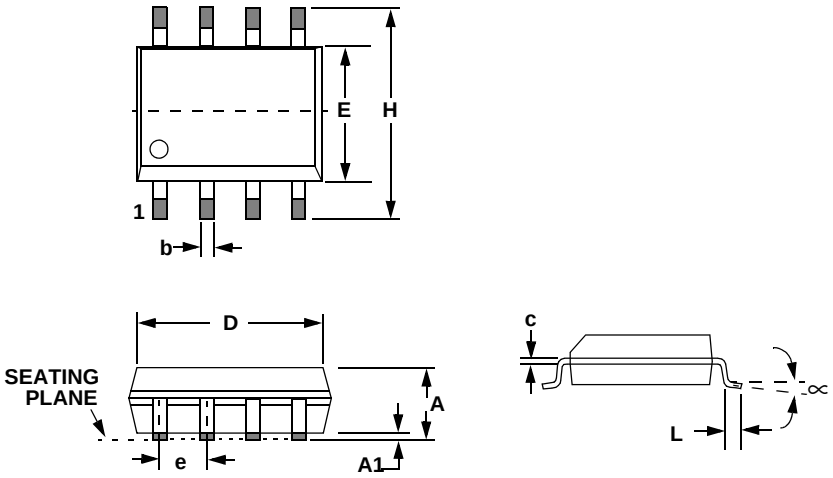
Figure 28. Overload — 240 mA to 500 mA, 265 VAC

6. DEFINITIONS

Variable	Definition
η	The efficiency factor.
α	A margin factor to guarantee rated power against tolerances and transients.
$f_{line(min)}$	The minimum AC line frequency.
I_{AC}	The current generated by V_{rect} that flows into the IAC pin.
I_{FB}	The current generated by V_{link} that flows into the FB pin.
$I_{FET(pk)}$	The PFC MOSFET peak current, which is equal to the peak current in the PFC boost inductor.
I_{rms}	The magnitude of the RMS current.
I_{sat}	The boost inductor L_B saturation current.
I_{st}	The sum of the current into the IAC and FB pins.
I_{ST}	The startup current of the chip.
L_B	The PFC boost inductor.
P_o	The nominal output power from the CS1500 PFC circuit.
$P_{o(max)}$	The maximum value of the output power from the CS1500 PFC circuit.
R_{AC}	The sense resistor used to measure current into the IAC pin.
R_{FB}	The sense resistor used to measure current into the FB pin.
$V_{in(min)}$	The minimum specified line voltage for proper operation (volts RMS).
V_{link}	The magnitude of the output voltage from the PFC.
$V_{link(min)}$	The magnitude of the output voltage from the PFC.
$\Delta V_{link(rip)}$	$\Delta V_{link(rip)}$, is the output voltage ripple requirement in volts peak-to-peak
V_{rect}	The instantaneous value of the rectified line voltage (volts).

7. PACKAGE DRAWING

8L SOIC (150 MIL BODY) PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.040	0.060	1.02	1.52
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
∝	0°	8°	0°	8°

JEDEC # MS-012

8. ORDERING INFORMATION

Part #	Temperature Range	Package Description
CS1500-FSZ	-40 °C to +125 °C	8-lead SOIC, Lead (Pb) Free

9. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating[a]	Max Floor Life[b]
CS1500-FSZ	260 °C	2	365 Days

a. MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

b. Stored at 30 °C, 60% relative humidity.

10.REVISION HISTORY

Revision	Date	Changes
A1	APR 2009	Initial Advance Information release.
A2	JUN 2009	No substantive changes. Document number incremented to avoid confusion among previous, pre-released versions.
A3	DEC 2009	Revised feature list & product description. Revised electrical characteristics to include brownout & open-loop protection. Modified definition table. Modified data sheet format.
A4	MAR 2010	Updated to correspond to C1 silicon.
A5	MAY 2010	Updated performance data.
A6	MAY 2010	Updated with additional test bench data for EP level.
A7	JUL 2010	Updated zener voltage, OPP threshold, brownout protection/recovery. Updated Fig.1 with new data.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to http://www.cirrus.com