Dual Channel, 14-Bit, 65 MSPS A/D Converter with Analog Input Signal Conditioning

AD10465

FEATURES

- **Dual, 65 MSPS minimum sample rate**
  - **Channel-to-channel matching, ±0.5% gain error**
  - **Channel-to-channel isolation, >90 dB**
  - **DC-coupled signal conditioning included**
- **Selectable bipolar input voltage range (±0.5 V, ±1.0 V, ±2.0 V)**
- **Gain flatness up to 25 MHz: <0.2 dB**
- **80 dB spurious-free dynamic range**
- **Twos complement output format**
- **3.3 V or 5 V CMOS-compatible output levels**
- **1.75 W per channel**
- **Industrial and military grade**

APPLICATIONS

- **Phased array receivers**
- **Communications receivers**
- **FLIR processing**
- **Secure communications**
- **GPS antijamming receivers**
- **Multichannel, multimode receivers**

GENERAL DESCRIPTION

The AD10465 is a full channel ADC solution with on-module signal conditioning for improved dynamic performance and fully matched channel-to-channel performance. The module includes two wide dynamic range AD6644 ADCs. Each AD6644 has a dc-coupled amplifier front end including an AD8037 low distortion, high bandwidth amplifier that provides high input impedance and gain and drives the AD8138 single-to-differential amplifier. The AD6644s have on-chip track-and-hold circuitry and utilize an innovative multipass architecture to achieve 14-bit, 65 MSPS performance.

The AD10465 uses innovative high density circuit design and laser trimmed, thin film resistor networks to achieve exceptional matching and performance, while still maintaining excellent isolation and providing for significant board area savings.

The AD10465 operates with ±5.0 V supplies for the analog signal conditioning with a separate 5.0 V supply for the analog-to-digital conversion and 3.3 V digital supply for the output stage. Each channel is completely independent, allowing operation with independent encode and analog inputs. The AD10465 also offers the user a choice of analog input signal ranges to further minimize additional external signal conditioning, while remaining general-purpose.

The AD10465 is packaged in a 68-lead ceramic leaded chip carrier package, footprint-compatible with the earlier generation AD10242 (12-bit, 40 MSPS) and AD10265 (12-bit, 65 MSPS). Manufacturing is done on the Analog Devices Mil-38534 Qualified Manufacturers Line (QML) and components are available up to Class-H (−40°C to +85°C). The AD6644 internal components are manufactured on Analog Devices' high speed complementary bipolar process (XFCB).

PRODUCT HIGHLIGHTS

1. Guaranteed sample rate of 65 MSPS.
2. Input amplitude options, user configurable.
3. Input signal conditioning included; both channels matched for gain.
4. Fully tested/characterized performance.
5. Footprint-compatible family; 68-lead CLCC package.

FUNCTIONAL BLOCK DIAGRAM

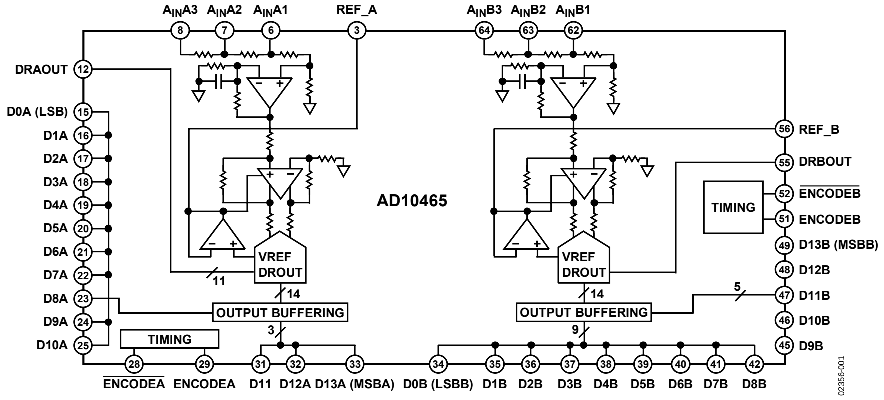

Figure 1.

Rev. A

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3/06—Rev. 0 to Rev. A

Remove AZ Grade	Universal
Changes to General Description Section	1
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2001—Revision 0: Initial Version

SPECIFICATIONS

AV_{CC} = +5 V; AV_{EE} = −5 V; DV_{CC} = 3.3 V applies to each ADC, unless otherwise noted. All specifications guaranteed within 100 ms of initial power-up, regardless of sequencing.

Table 1.

		Test[1]	Mil	AD10465BZ/QML-H			
Parameter	**Temp**	**Level**	**Subgroup**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION					14		Bits
DC ACCURACY							
No Missing Codes	Full	VI	1, 2, 3		Guaranteed		
Offset Error	25°C	I	1	−2.2	±0.02	+2.2	% FS
	Full	VI	2, 3	−2.2	±1.0	+2.2	% FS
Offset Error Channel Match	Full	V		−1	±1.0	+1	%
Gain Error[2]	25°C	I	1	−3	−1.0	+1	% FS
	Full	VI	2, 3	−5	±2.0	+5	% FS
Gain Error Channel Match	25°C	I	1	−1.5	±0.5	+1.5	%
	Max	I	2	−3	±1.0	+3	%
	Min	I	3	−5		+5	%
ANALOG INPUT (A_{IN})							
Input Voltage Range							
$A_{IN}1$	Full	V			±0.5		V
$A_{IN}2$	Full	V			±1.0		V
$A_{IN}3$	Full	V			±2		V
Input Resistance							
$A_{IN}1$	Full	IV	12	99	100	101	Ω
$A_{IN}2$	Full	IV	12	198	200	202	Ω
$A_{IN}3$	Full	IV	12	396	400	404	Ω
Input Capacitance[3]	25°C	IV	12	0	4.0	7.0	pF
Analog Input Bandwidth[4]	Full	V			100		MHz
ENCODE INPUT (ENC, $\overline{ENC}$)[5]							
Differential Input Voltage	Full	IV		0.4			V p-p
Differential Input Resistance	25°C	V			10		kΩ
Differential Input Capacitance	25°C	V			2.5		pF
SWITCHING PERFORMANCE							
Maximum Conversion Rate[6]	Full	VI	4, 5, 6	65			MSPS
Minimum Conversion Rate[6]	Full	V	12			20	MSPS
Aperture Delay (t_A)	25°C	V			1.5		ns
Aperture Delay Matching	25°C	IV	12		250	500	ps
Aperture Uncertainty (Jitter)	25°C	V			0.3		ps rms
ENCODE Pulse Width High	25°C	IV	12	6.2	7.7	9.2	ns
ENCODE Pulse Width Low	25°C	IV	12	6.2	7.7	9.2	ns
Output Delay (t_{OD})	Full	V			6.8		ns
ENCODE, Rising to Data Ready, Rising Delay (T_{E_DR})	Full				11.5		ns
SNR[7]							
Analog Input @ 4.98 MHz	25°C	V			70		dBFS
Analog Input @ 9.9 MHz	25°C	I	4	69	70		dBFS
	Full	II	5, 6	68	70		dBFS
Analog Input @ 19.5 MHz	25°C	I	4	68	70		dBFS
	Full	II	5, 6	67	70		dBFS
Analog Input @ 32.1 MHz	25°C	I	4	67	69		dBFS
	Full	II	5, 6	67	69		dBFS

		Test[1]	Mil	AD10465BZ/QML-H			
Parameter	**Temp**	**Level**	**Subgroup**	**Min**	**Typ**	**Max**	**Unit**
SINAD[8]							
Analog Input @ 4.98 MHz	25°C	V			70		dB
Analog Input @ 9.9 MHz	25°C	I	4	67.5	69		dB
	Full	II	5, 6	67.5	69		dB
Analog Input @ 19.5 MHz	25°C	I	4	65	68		dB
	Full	II	5, 6	65	68		dB
Analog Input @ 32.1 MHz	25°C	I	4	60	63		dB
	Full	II	5, 6	58	61		dB
SPURIOUS-FREE DYNAMIC RANGE[9]							
Analog Input @ 4.98 MHz	25°C	V			85		dBFS
Analog Input @ 9.9 MHz	25°C	I	4	73	82		dBFS
	Full	II	5, 6	70	82		dBFS
Analog Input @ 19.5 MHz	25°C	I	4	72	78		dBFS
	Full	II	5, 6	70	78		dBFS
Analog Input @ 32.1 MHz	25°C	I	4	62	68		dBFS
	Full	II	5, 6	60	66		dBFS
TWO-TONE IMD REJECTION[10]							
f_{IN} = 10 MHz and 11 MHz	25°C	I	4	78	87		dBFS
f_1 and f_2 are −7 dB		II	5, 6	78			dBFS
f_{IN} = 31 MHz and 32 MHz	25°C	I	4	68	70		dBFS
f_1 and f_2 Are −7 dB	Full	II	5, 6	60			dBFS
CHANNEL-TO-CHANNEL ISOLATION[11]	25°C	IV	12		90		dB
TRANSIENT RESPONSE	25°C	V			15.3		ns
OVERVOLTAGE RECOVERY TIME							
VIN = 2.0 × f_S	Full	IV	12		40	100	ns
VIN = 4.0 × f_S	Full	IV	12		150	200	ns
DIGITAL OUTPUTS[12]							
Logic Compatibility					CMOS		
DV_{CC} = 3.3 V							
Logic 1 Voltage	Full	I	1, 2, 3	2.5	DV_{CC} − 0.2		V
Logic 0 Voltage	Full	I	1, 2, 3		0.2	0.5	V
DV_{CC} = 5 V							
Logic 1 Voltage	Full	V			DV_{CC} − 0.3		V
Logic 0 Voltage	Full	V			0.35		V
Output Coding				Twos complement			
POWER SUPPLY							
AV_{CC} Supply Voltage[13]	Full	VI		4.85	5.0	5.25	V
I (AV_{CC}) Current	Full	I			270	308	mA
AV_{EE} Supply Voltage[13]	Full	VI		−5.25	−5.0	−4.75	V
I (AV_{EE}) Current	Full	V			38	49	mA
DV_{CC} Supply Voltage[13]	Full	VI		3.135	3.3	3.465	V
I (DV_{CC}) Current	Full	V			30	46	mA
I_{CC} (Total) Supply Current per Channel	Full	I	1, 2, 3		338	403	mA
Power Dissipation (Total)	Full	I	1, 2, 3		3.5	3.9	W
Power Supply Rejection Ratio (PSRR)	Full	V			0.02		% FSR/% V_S
Passband Ripple to 10 MHz		V			0.1		dB
Passband Ripple to 25 MHz		V			0.2		dB

[1] See Table 3.

[2] Gain tests are performed on $A_{IN}1$ input voltage range.

[3] Input capacitance specification combines AD8037 die capacitance and ceramic package capacitance.

[4] Full power bandwidth is the frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

[5] All ac specifications tested by driving $\overline{\text{ENCODE}}$ and ENCODE differentially.

[6] Minimum and maximum conversion rates allow for variation in encode duty cycle of 50% ± 5%.

[7] Analog input signal power at −1 dBFS; signal-to-noise ratio (SNR) is the ratio of signal level to total noise (first five harmonics removed). ENCODE = 65 MSPS. SNR is reported in dBFS, related back to converter full power.

[8] Analog input signal power at −1 dBFS. Signal-to-noise and distortion (SINAD) is the ratio of signal level to total noise + harmonics. ENCODE = 65 MSPS.

[9] Analog input signal power swept from −1 dBFS to −60 dBFS; SFDR is the ratio of converter full scale to worst spur.

[10] Both input tones at −7 dBFS; two-tone intermodulation distortion (IMD) rejection is the ratio of either tone to the worst third order intermodulation product.

[11] Channel-to-channel isolation tested with A channel grounded and a full-scale signal applied to B channel.

[12] Digital output logic levels: $DV_{CC} = 3.3$ V, $C_{LOAD} = 10$ pF. Capacitive loads > 10 pF degrade performance.

[13] Supply voltage recommended operating range. AV_{CC} can be varied from 4.85 V to 5.25 V. However, rated ac (harmonics) performance is valid only over the range $AV_{CC} = 5.0$ V to 5.25 V.

TEST CIRCUITS

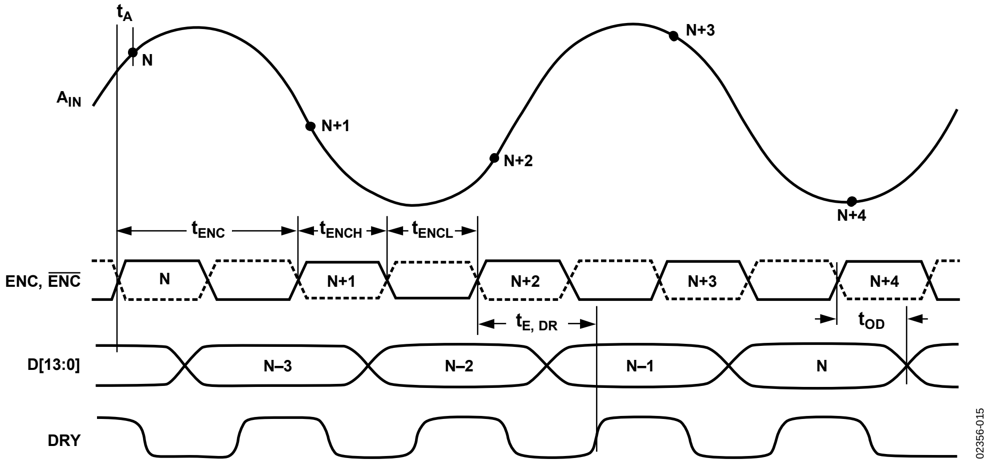


Figure 2. Timing Diagram

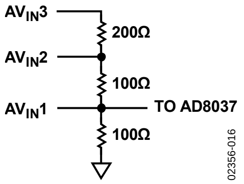


Figure 3. Analog Input Stage

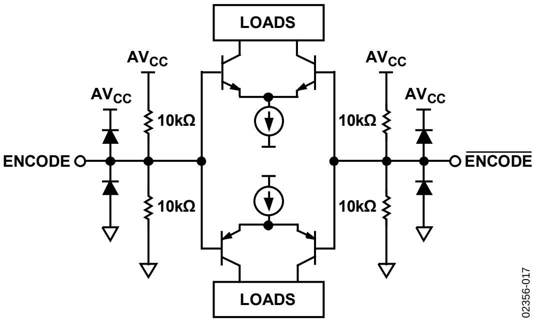


Figure 4. ENCODE Inputs

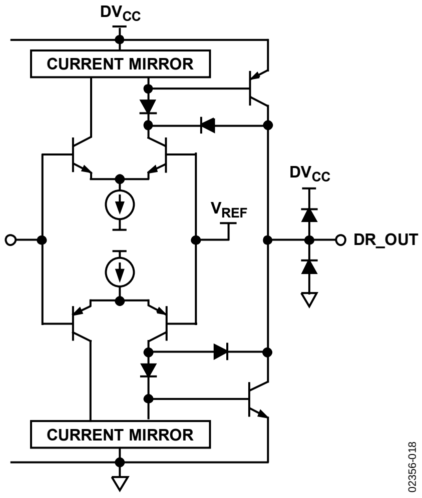


Figure 5. Digital Output Stage

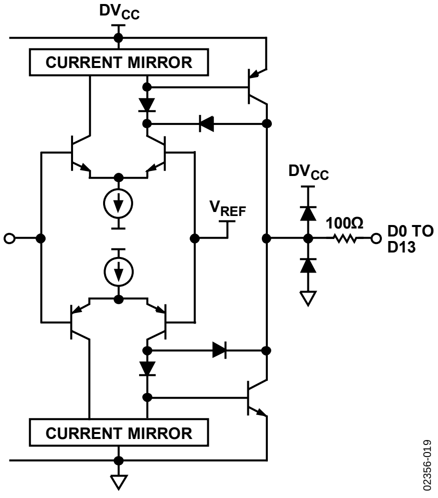


Figure 6. Digital Output Stage

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Min	Max	Units
ELECTRICAL			
V_{CC} Voltage	0	+7	V
V_{EE} Voltage	−7	0	V
Analog Input Voltage	V_{EE}	V_{CC}	V
Analog Input Current	−10	+10	mA
Digital Input Voltage (ENCODE)	0	V_{CC}	V
ENCODE, $\overline{\text{ENCODE}}$ Differential Voltage		4	V
Digital Output Current	−10	+10	mA
ENVIRONMENTAL[1]			
Operating Temperature Range (Case)	−40	+85	°C
Maximum Junction Temperature		174	°C
Lead Temperature (Soldering, 10 sec)		300	°C
Storage Temperature Range (Ambient)	−65	+150	°C

[1] Typical thermal impedance for 68-lead CLCC package: θ_{JC} = 2.2°C/W; θ_{JA} = 24.3°C/W.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Test Levels

Level	Description
I	100% production tested.
II	100% production tested at 25°C, and sample tested at specified temperatures. AC testing done on sample basis.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	100% production tested at 25°C, sample tested at temperature extremes.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND PIN FUNCTION DESCRIPTIONS

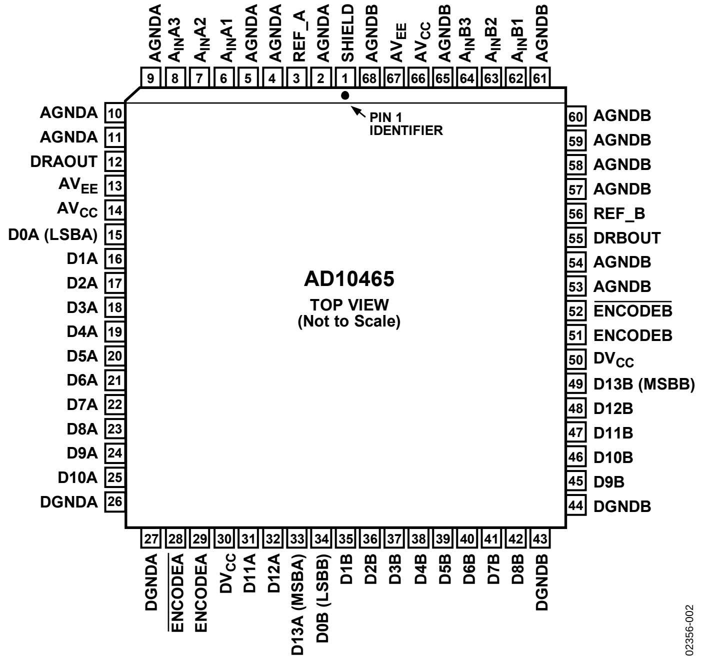


Figure 7. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SHIELD	Internal Ground Shield Between Channels.
2, 4, 5, 9 to11	AGNDA	A Channel Analog Ground. A ground and B ground should be connected as close to the device as possible.
3	REF_A	A Channel Internal Voltage Reference.
6	$A_{IN}A1$	Analog Input for A Side ADC (Nominally ±0.5 V).
7	$A_{IN}A2$	Analog Input for A Side ADC (Nominally ±1.0 V).
8	$A_{IN}A3$	Analog Input for A Side ADC (Nominally ±2.0 V).
12	DRAOUT	Data Ready A Output.
13	AV_{EE}	Analog Negative Supply Voltage (Nominally −5.0 V or −5.2 V).
14	AV_{CC}	Analog Positive Supply Voltage (Nominally 5.0 V).
26, 27	DGNDA	A Channel Digital Ground.
15 to 25, 31 to 33	D0A to D13A	Digital Outputs for ADC A. D0A (LSBA).
28	$\overline{\text{ENCODEA}}$	Complement of ENCODE.
29	ENCODEA	Data Conversion Initiated on Rising Edge of ENCODE Input.
30	DV_{CC}	Digital Positive Supply Voltage (Nominally 5.0 V or 3.3 V).
43, 44	DGNDB	B Channel Digital Ground.
34 to 42, 45 to 49	D0B to D13B	Digital Outputs for ADC B. D0B (LSBB).
53, 54, 57 to 61, 65, 68	AGNDB	B Channel Analog Ground. A ground and B ground should be connected as close to the device as possible.
50	DV_{CC}	Digital Positive Supply Voltage (Nominally 5.0 V or 3.3 V).
51	ENCODEB	Data conversion initiated on rising edge of ENCODE input.
52	$\overline{\text{ENCODEB}}$	Complement of ENCODEB.
55	DRBOUT	Data Ready B Output.
56	REF_B	B Channel Internal Voltage Reference.
62	$A_{IN}B1$	Analog Input for B Side ADC (Nominally ±0.5 V).
63	$A_{IN}B2$	Analog Input for B Side ADC (Nominally ±1.0 V).
64	$A_{IN}B3$	Analog Input for B Side ADC (Nominally ±2.0 V).
66	AV_{CC}	Analog Positive Supply Voltage (Nominally 5.0 V).
67	AV_{EE}	Analog Negative Supply Voltage (Nominally −5.0 V or −5.2 V).

TYPICAL PERFORMANCE CHARACTERISTICS

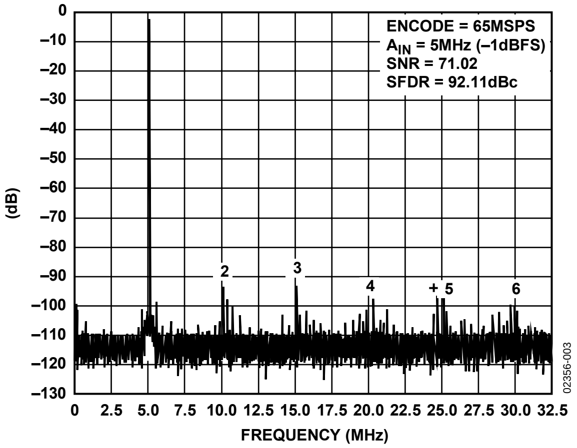


Figure 8. Single Tone @ 5 MHz

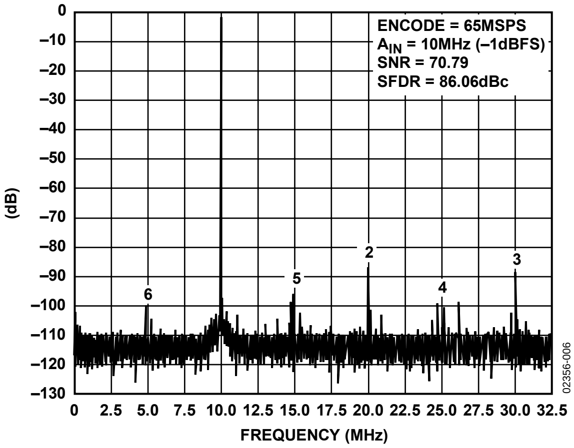


Figure 11. Single Tone @ 10 MHz

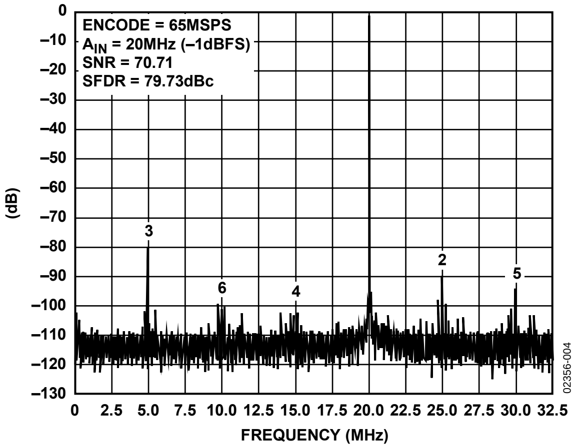


Figure 9. Single Tone @ 20 MHz

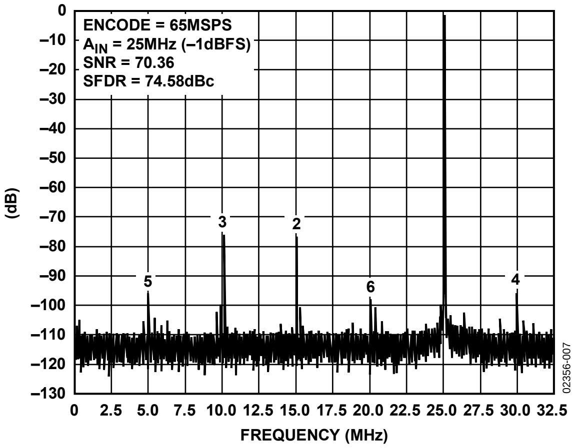


Figure 12. Single Tone @ 25 MHz

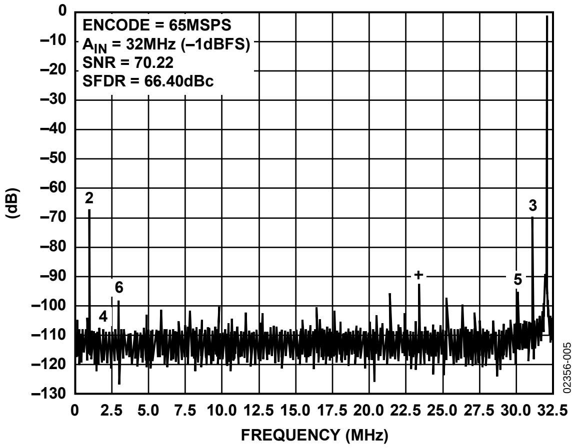


Figure 10. Single Tone @ 32 MHz

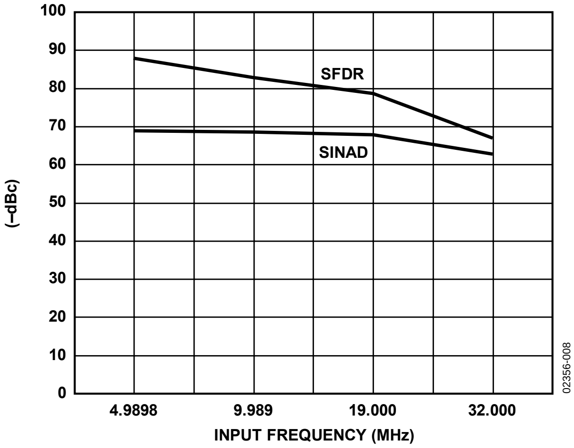


Figure 13. SFDR and SINAD vs. Frequency

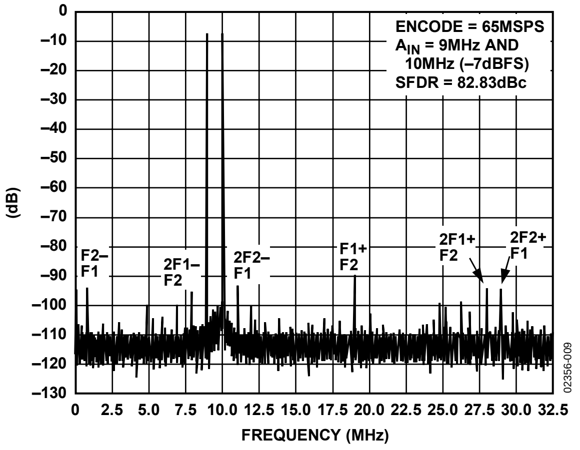


Figure 14. Two Tone @ 9 MHz and 10 MHz

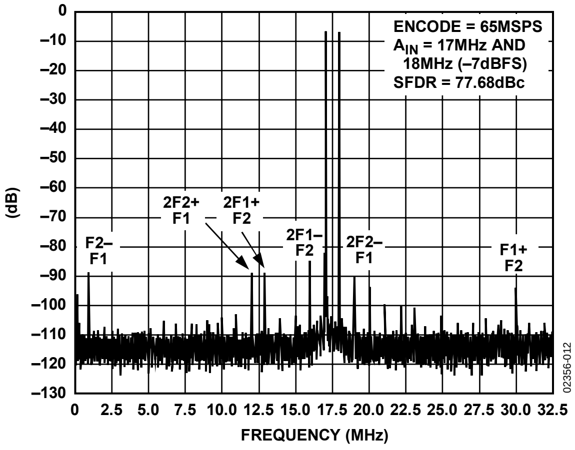


Figure 17. Two Tone @ 17 MHz and 18 MHz

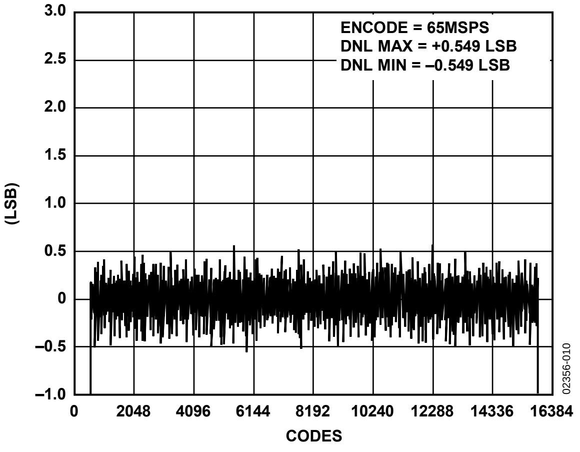


Figure 15. Differential Nonlinearity

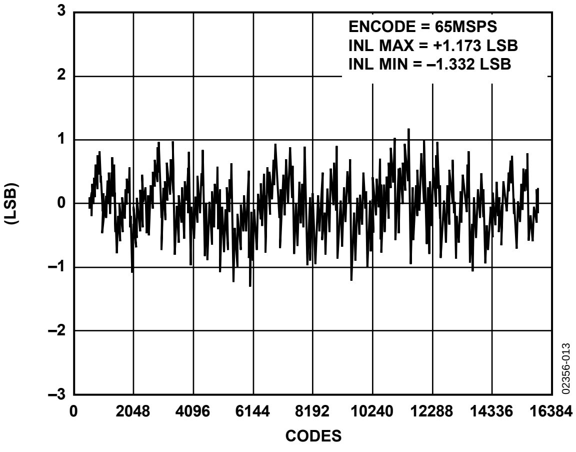


Figure 18. Integral Nonlinearity

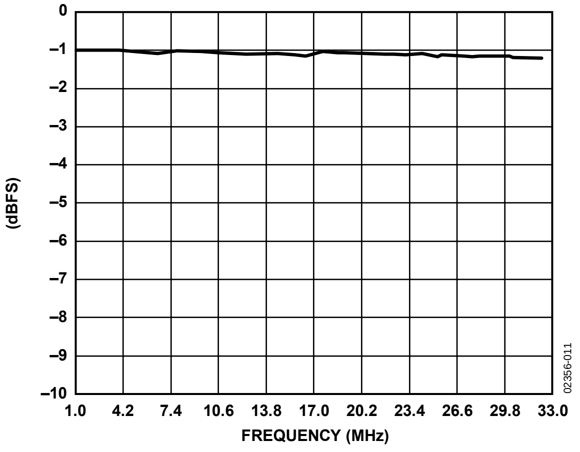


Figure 16. Gain Flatness

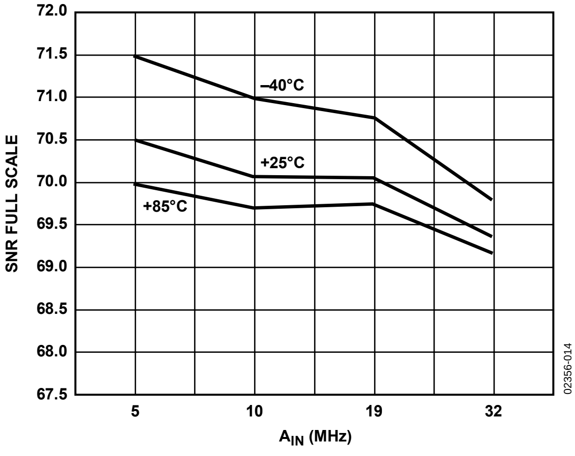


Figure 19. SNR vs. A_{IN} Frequency

TERMINOLOGY

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between a differential crossing of ENCODE and $\overline{\text{ENCODE}}$, and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

ENCODE Pulse Width/Duty Cycle
Pulse width high is the minimum amount of time that the ENCODE pulse should be left in Logic 1 state to achieve rated performance; pulse width low is the minimum time ENCODE pulse should be left in low state. At a given clock rate, these specs define an acceptable encode duty cycle.

Harmonic Distortion
The ratio of the rms signal amplitude to the rms value of the worst harmonic component.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed, above which converter performance can degrade.

Output Propagation Delay
The delay between a differential crossing of ENCODE and $\overline{\text{ENCODE}}$, and the time when all output data bits are within valid logic levels.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 0.02% accuracy after an analog input signal of the specified percentage of full scale is reduced to midscale.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise and Distortion (SINAD)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc. Can be reported in dB (that is, relative to signal level) or in dBFS (always related back to converter full scale).

Signal-to-Noise Ratio (Without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc. Can be reported in dB (that is, relative to signal level) or in dBFS (always related back to converter full scale).

Spurious-Free Dynamic Range
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic.

Transient Response
The time required for the converter to achieve 0.03% accuracy when a one-half, full-scale step function is applied to the analog input.

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third-order intermodulation product; reported in dBFS.

THEORY OF OPERATION

The AD10465 is a high dynamic range, 14-bit, 65 MHz pipeline delay (three pipelines) analog-to-digital converter. The custom analog input section maintains the same input ranges (1 V p-p, 2 V p-p, and 4 V p-p) and input impedance (100 Ω, 200 Ω, and 400 Ω) as the AD10242.

The AD10465 employs four monolithic Analog Devices components per channel (AD8037, AD8138, AD8031, and AD6644), along with multiple passive resistor networks and decoupling capacitors to fully integrate a complete 14-bit analog-to-digital converter.

The input signal is passed through a precision laser trimmed resistor divider allowing the user to externally select operation with a full-scale signal of ±0.5 V, ±1.0 V, or ±2.0 V by choosing the proper input terminal for the application.

The AD10465 analog input includes an AD8037 amplifier featuring an innovative architecture that maximizes the dynamic range capability on the amplifiers inputs and outputs. The AD8037 amplifier provides a high input impedance and gain for driving the AD8138 in a single-ended to differential amplifier configuration. The AD8138 has a −3 dB bandwidth at 300 MHz and delivers a differential signal with the lowest harmonic distortion available in a differential amplifier. The AD8138 differential outputs help balance the differential inputs to the AD6644, maximizing the performance of the ADC.

The AD8031 provides the buffer for the internal reference of the AD6644. The internal reference voltage of the AD6644 is designed to track the offsets and drifts of the ADC and is used to ensure matching over an extended temperature range of operation. The reference voltage is connected to the output common-mode input on the AD8138. The AD6644 reference voltage sets the output common mode on the AD8138 at 2.4 V, which is the midsupply level for the AD6644.

The AD6644 has complementary analog input pins, AIN and $\overline{\text{AIN}}$. Each analog input is centered at 2.4 V and should swing ±0.55 V around this reference. Since AIN and $\overline{\text{AIN}}$ are 180° out of phase, the differential analog input signal is 2.2 V peak-to-peak. Both analog inputs are buffered prior to the first track-and-hold, TH1. The high state of the ENCODE pulse places TH1 in hold mode. The held value of TH1 is applied to the input of a 5-bit coarse ADC1. The digital output of ADC1 drives 14 bits of precision, which is achieved through laser trimming. The output of DAC1 is subtracted from the delayed analog signal at the input of TH3 to generate a first residue signal. TH2 provides an analog pipeline delay to compensate for the digital delay of ADC1.

The first residue signal is applied to a second conversion stage consisting of a 5-bit ADC2, 5-bit DAC2, and pipeline TH4. The second DAC requires 10 bits of precision, which is met by the process with no trim. The input to TH5 is a second residue signal generated by subtracting the quantized output of DAC2 from the first residue signal held by TH4. TH5 drives a final 6-bit ADC3.

The digital outputs from ADC1, ADC2, and ADC3 are added together and corrected in the digital error correction logic to generate the final output data. The result is a 14-bit parallel digital CMOS-compatible word, coded as twos complement.

USING THE FLEXIBLE INPUT

The AD10465 has been designed with the user's ease of operation in mind. Multiple input configurations have been included on board to allow the user a choice of input signal levels and input impedance. While the standard inputs are ±0.5 V, ±1.0 V, and ±2.0 V, the user can select the input impedance of the AD10465 on any input by using the other inputs as alternate locations for GND or an external resistor. Table 5 summarizes the impedance options available at each input location.

Table 5. Input Impedance Options

Input	Impedance	Condition
$A_{IN}1$	100 Ω	When $A_{IN}2$ and $A_{IN}3$ are open
	75 Ω	When $A_{IN}3$ is shorted to GND
	50 Ω	When $A_{IN}2$ is shorted to GND
$A_{IN}2$	200 Ω	When $A_{IN}3$ is open
	100 Ω	When $A_{IN}3$ is shorted to GND
	75 Ω	When $A_{IN}2$ to $A_{IN}3$ has an external resistor of 300 Ω, with $A_{IN}3$ shorted to GND
	50 Ω	When $A_{IN}2$ to $A_{IN}3$ has an external resistor of 100 Ω, with $A_{IN}3$ shorted to GND
$A_{IN}3$	400 Ω	
	100 Ω	When $A_{IN}3$ has an external resistor of 133 Ω to GND
	75 Ω	When $A_{IN}3$ has an external resistor of 92 Ω to GND
	50 Ω	When $A_{IN}3$ has an external resistor of 57 Ω to GND

APPLYING THE AD10465

ENCODING THE AD10465

The AD10465 encode signal must be a high quality, extremely low phase noise source to prevent degradation of performance. Maintaining 14-bit accuracy places a premium on encode clock phase noise. SNR performance can easily degrade by 3 dB to 4 dB with 32 MHz input signals when using a high jitter clock source. See the Analog Devices Application Note AN-501, *Aperture Uncertainty and ADC System Performance*, for complete details. For optimum performance, the AD10465 must be clocked differentially. The encode signal is usually ac-coupled into the ENCODE and $\overline{\text{ENCODE}}$ pins via a transformer or capacitors. These pins are biased internally and require no additional bias.

Figure 20 shows one preferred method for clocking the AD10465. The clock source (low jitter) is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD10465 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to the other portions of the AD10465, and limits the noise presented to the ENCODE inputs. A crystal clock oscillator can also be used to drive the RF transformer if an appropriate limiting resistor (typically 100 Ω) is placed in the series with the primary.

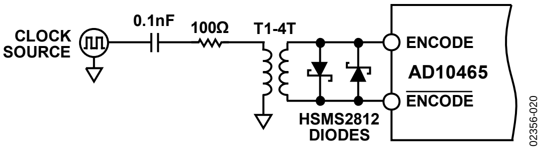


Figure 20. Crystal Clock Oscillator, Differential ENCODE

If a low jitter ECL/PECL clock is available, another option is to ac couple a differential ECL/PECL signal to the ENCODE and $\overline{\text{ENCODE}}$ input pins as shown in Figure 21. A device that offers excellent jitter performance is the MC100LVEL16 (or same family) from Motorola.

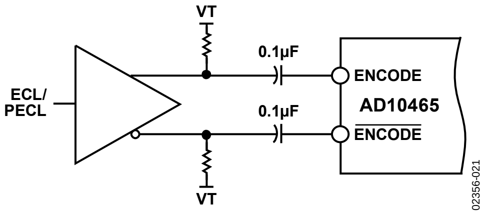


Figure 21. Differential ECL for ENCODE

JITTER CONSIDERATIONS

The signal-to-noise ratio (SNR) for an ADC can be predicted. When normalized to ADC codes, Equation 1 accurately predicts the SNR based on three terms. These are jitter, average DNL error, and thermal noise. Each of these terms contributes to the noise within the converter.

$$SNR = -20 \times \log \left[\left(\frac{1+\varepsilon}{2^N}\right) + \left(2 \times \pi \times f_{ANALOG} \times t_j\ rms\right)^2 + \left(\frac{v_{NOISE\ rms}}{2^n}\right)^2 \right]^{1/2} \quad (1)$$

where:

f_{ANALOG} is the analog input frequency.

$t_{j\ rms}$ is the rms jitter of the encode (rms sum of encode source and internal encode circuitry).

ε is the average DNL of the ADC (typically 0.50 LSB).

N is the number of bits in the ADC.

$V_{NOISE\ rms}$ is the V rms noise referred to the analog input of the ADC (typically 5 LSB).

For a 14-bit analog-to-digital converter like the AD10465, aperture jitter can greatly affect the SNR performance as the analog frequency is increased. The chart below shows a family of curves that demonstrates the expected SNR performance of the AD10465 as jitter increases. The chart is derived from Equation 1.

For a complete discussion of aperture jitter, please consult the Analog Devices Application Note AN-501, *Aperture Uncertainty and ADC System Performance.*

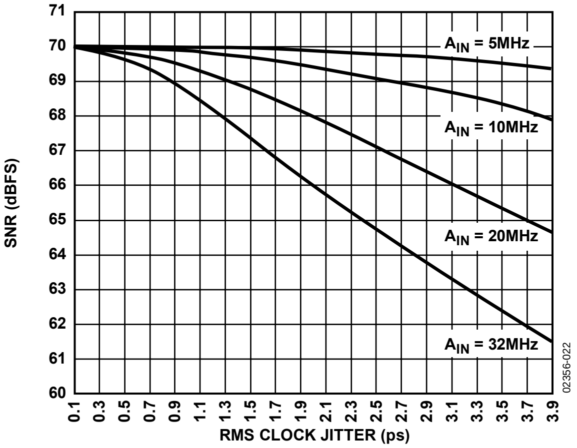


Figure 22. SNR vs. Jitter

POWER SUPPLIES

Care should be taken when selecting a power source. Linear supplies are strongly recommended. Switching supplies tend to have radiated components that can be "received" by the AD10465. Each of the power supply pins should be decoupled as closely to the package as possible using 0.1 µF chip capacitors.

The AD10465 has separate digital and analog power supply pins. The analog supplies are denoted AV_{CC} and the digital supply pins are denoted DV_{CC}. AV_{CC} and DV_{CC} should be separate power supplies. This is because the fast digital output swings can couple switching current back into the analog supplies. Note that AV_{CC} must be held within 5% of 5 V. The AD10465 is specified for DV_{CC} = 3.3 V as this is a common supply for digital ASICs.

OUTPUT LOADING

Care must be taken when designing the data receivers for the AD10465. The digital outputs drive an internal series resistor (for example, 100 Ω) followed by a gate, such as the 75LCX574. To minimize capacitive loading, there should only be one gate on each output pin. An example of this is shown in the evaluation board schematic shown in Figure 26. The digital outputs of the AD10465 have a constant output slew rate of 1 V/ns. A typical CMOS gate combined with a PCB trace has a load of approximately 10 pF. Therefore, as each bit switches, 10 mA (10 pF × 1 V ÷1 ns) of dynamic current per bit flows in or out of the device. A full-scale transition can cause up to 140 mA (14 bits ×10 mA/bit) of current flow through the output stages. These switching currents are confined between ground and the DV_{CC} pin. Standard TTL gates should be avoided because they can appreciably add to the dynamic switching currents of the AD10465. It should also be noted that extra capacitive loading increases output timing and invalidates timing specifications. Digital output timing is guaranteed with 10 pF loads.

LAYOUT INFORMATION

The schematic of the evaluation board (see Figure 24) represents a typical implementation of the AD10465. The pinout of the AD10465 is very straightforward and facilitates ease of use and the implementation of high frequency/high resolution design practices. It is recommended that high quality ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. All capacitors can be standard high quality ceramic chip capacitors.

Care should be taken when placing the digital output runs. Because the digital outputs have such a high slew rate, the capacitive loading on the digital outputs should be minimized. Circuit traces for the digital outputs should be kept short and connect directly to the receiving gate. Internal circuitry buffers the outputs of the ADC through a resistor network to eliminate the need to externally isolate the device from the receiving gate.

EVALUATION BOARD

The AD10465 evaluation board (Figure 23) is designed to provide optimal performance for evaluation of the AD10465 analog-to-digital converter. The board encompasses everything needed to ensure the highest level of performance for evaluating the AD10465. The board requires an analog input signal, encode clock, and power supply inputs. The clock is buffered on-board to provide clocks for the latches. The digital outputs and clocks are available at the standard 40-pin connectors, Connector J1 and Connector J2.

Power to the analog supply pins is connected via banana jacks. The analog supply powers the associated components and the analog section of the AD10465. The digital outputs of the AD10465 are powered via banana jacks with 3.3 V. Contact the factory if additional layout or applications assistance is required.

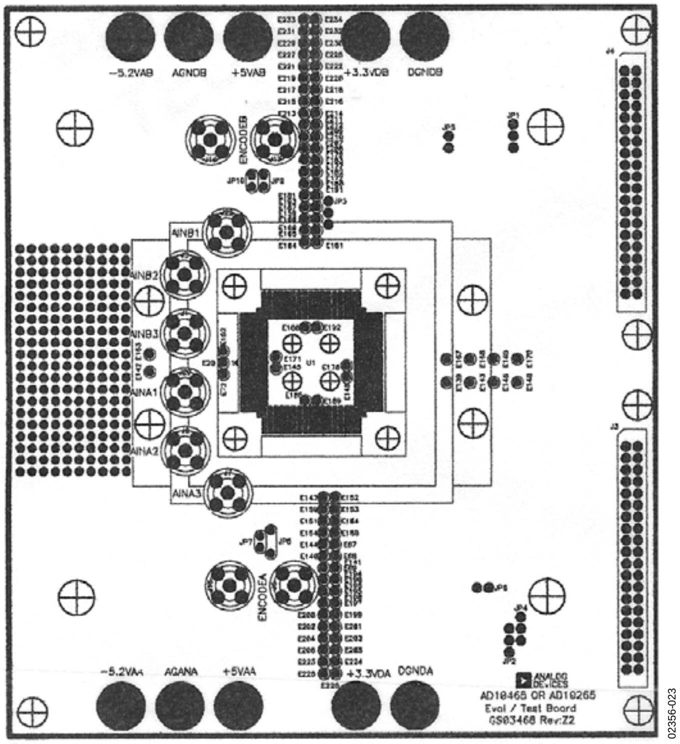


Figure 23. Evaluation Board Mechanical Layout

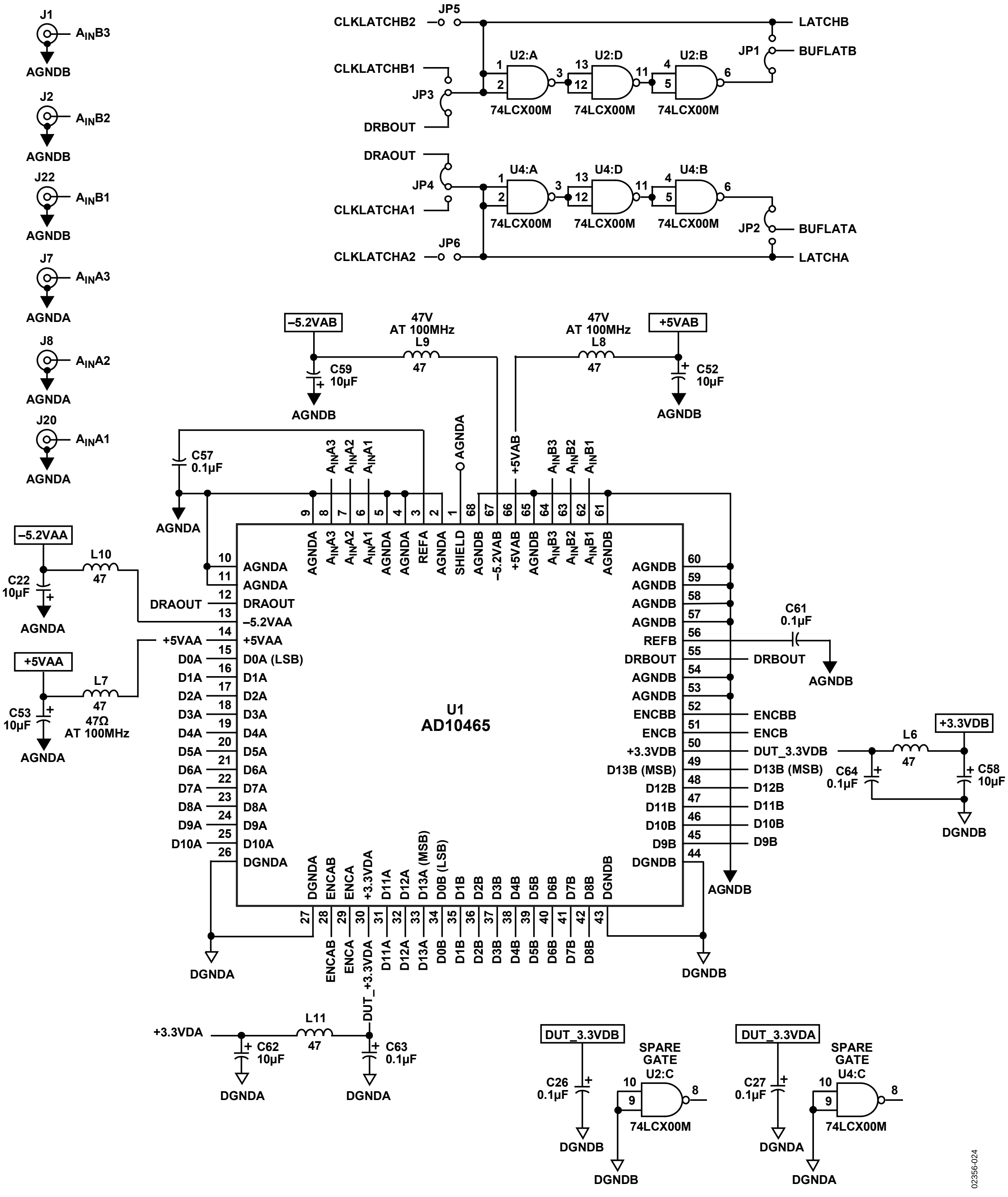


Figure 24. Evaluation Board

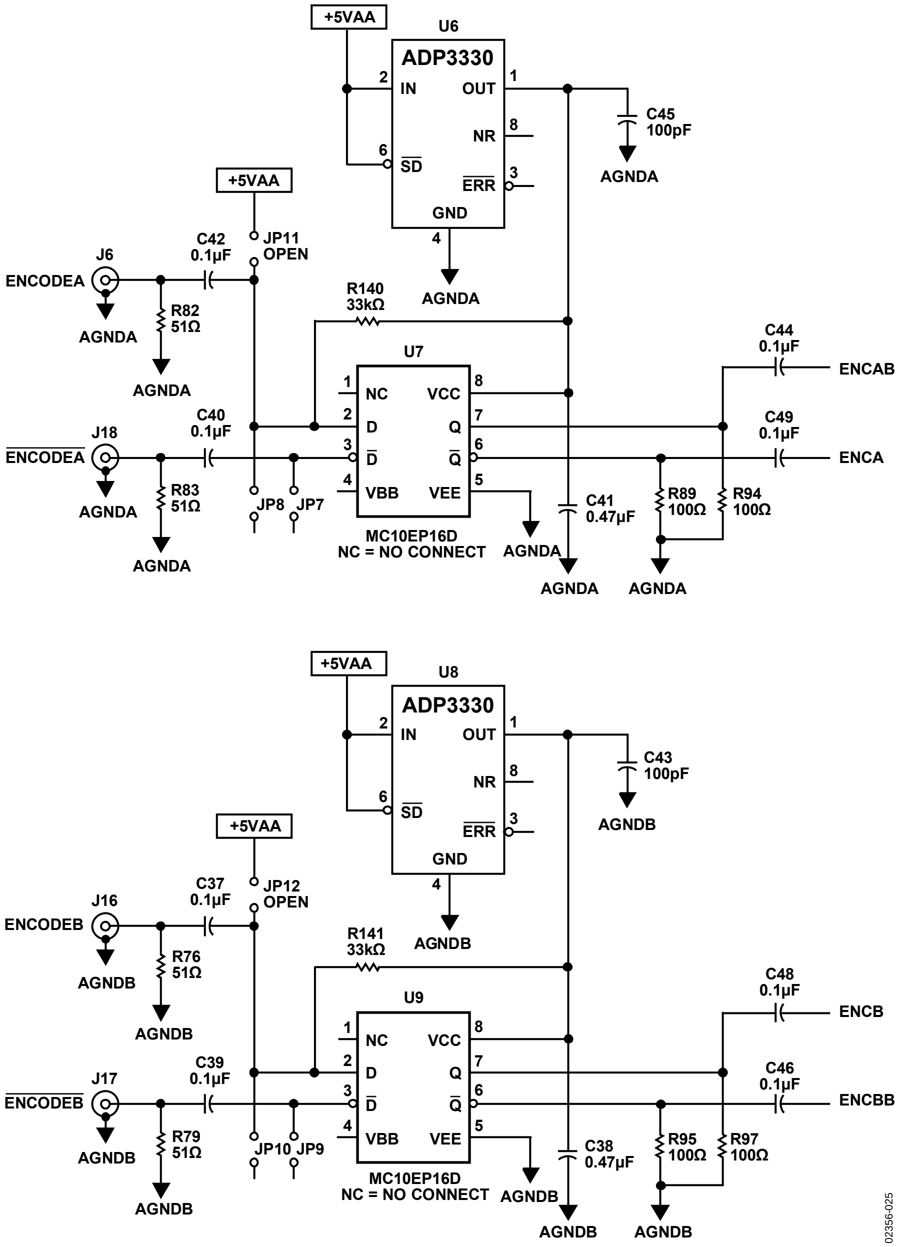


Figure 25. Evaluation Board

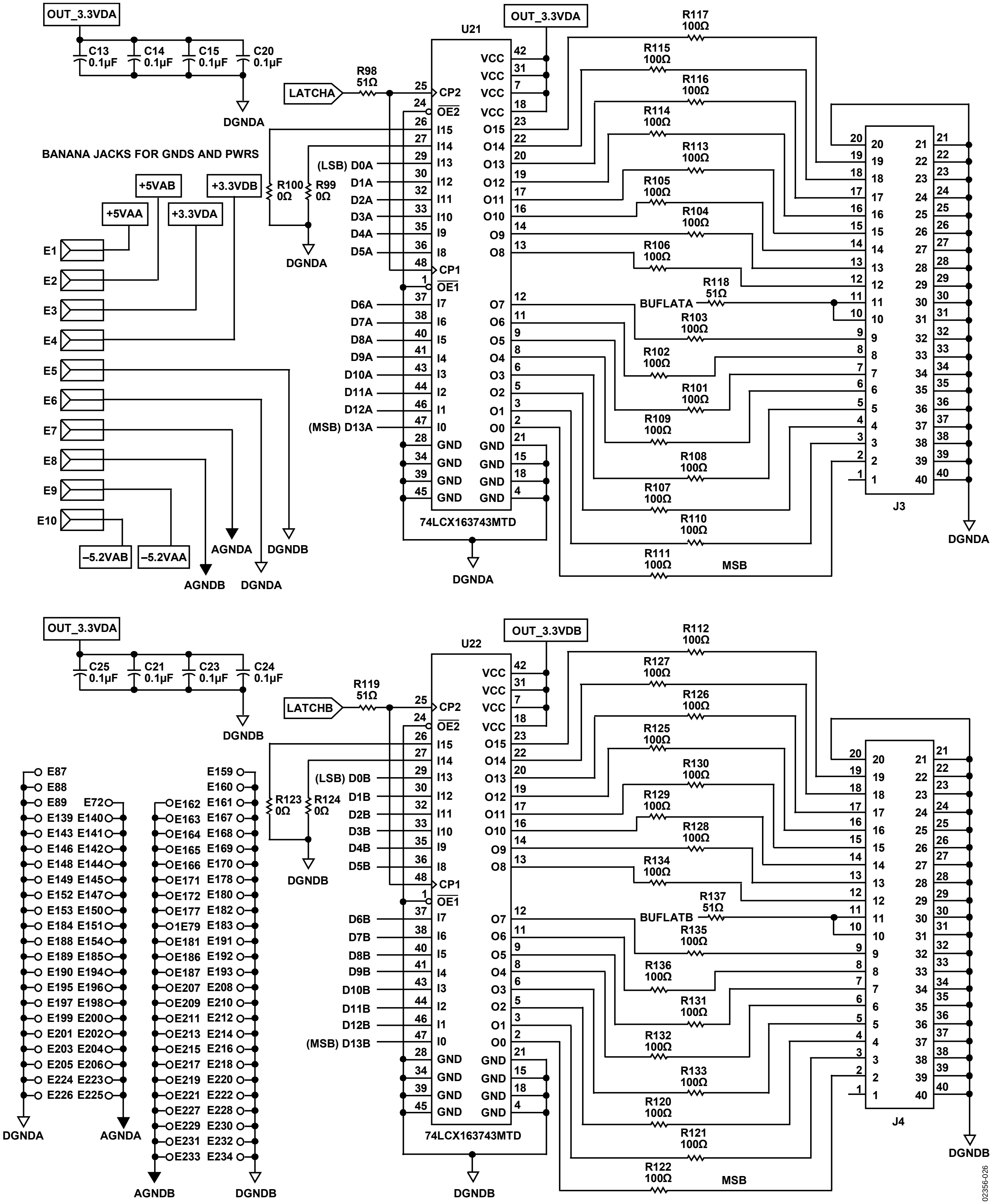


Figure 26. Evaluation Board

BILL OF MATERIALS LIST FOR AD10465 EVALUATION BOARD

Table 6. Bill of Materials

Qty	Reference Designator	Value	Description	Manufacturer and Part Number	Component Name
2	U2, U4		IC, low-voltage Quad 2-input nand, SOIC-14	Toshiba/TC74LCX00FN	74LCX00M
2	U21, U22		IC, 16-bit transparent latch with three-state outputs, TSSOP-48	Fairchild/74LCX163743MTD	74LCX163743MTD
1	U1		DUT, IC 14-bit analog-to-digital converter	ADI/AD10465BZ	ADI/AD10465BZ
2	U6, U8		IC, voltage regulator 3.3 V, RT-6	Analog Devices/ADP3330ART-3, 3-RLT	ADP3330
10	E1 to E10		Banana jack, socket	Johnson Components/08-0740-001	Banana Hole
22	C13 to C15, C20, C21, C23 to C27, C37, C39, C40, C42, C44, C46, C48, C49, C57, C61, C63, C64	0.1 µF	Capacitor, 0.1 µF, 20%, 12 V dc, 0805	Mena/GRM40X7R104K025BL	CAP 0805
2	C38, C41	0.47 µF	Capacitor, 0.47 µF, 5%, 12 V dc, 1206	Vitramon/VJ1206U474MFXMB	CAP 1206
2	C43, C45	100 pF	Capacitor, 100 pF, 10%, 12 V dc, 0805	Johansen/500R15N101JV4	CAP 0805
2	J3, J4		Connector, 40-pin header male	Samtec/TSW-120-08-G-D	HD40M
6	L6 to L11	47 µH	Inductor, 47 µH @ 100 MHz, 20%, IND2	Fair-Rite/2743019447	IND2
2	U7, U9		IC, differential receiver, SOIC-8	Motorola/MC10EP16D	MC10EP16D
6	C22, C52, C53, C58, C59, C62	10 µF	Capacitor, 10 µF, 20%, 16 V dc, 1812POL	Kemet/T491C106M016A57280	POLCAP 1812
4	R99, R100, R123, R124	0.0 Ω	Resistor, 0.0 Ω, 0805	Panasonic/ERJ-6GEY0R00V	RES2 0805
2	R140, R141	33,000 Ω	Resistor, 33,000 Ω, 5%, 0.10 Watt, 0805	Panasonic/ERJ-6GEYJ333V	RES2 0805
8	R76, R79, R82, R83, R98, R118, R119, R137	51 Ω	Resistor, 51 Ω, 5%, 0.10 Watt, 0805	Panasonic/ERJ-6GEYJ510V	RES2 0805, RES 0805
36	R89, R94, R95, R97, R101 to R117, R120 to R122, R125 to R136	100 Ω	Resistor, 100 Ω, 5%, 0.10 Watt, 0805	Panasonic/ERJ-6GEYJ101V	RES2 0805, RES 0805
8	J1, J2, J6 to J8, J16 to J18, J20, J22		Connector, SMA female	Johnson Components/142-0701-201	SMA

SILKSCREENS

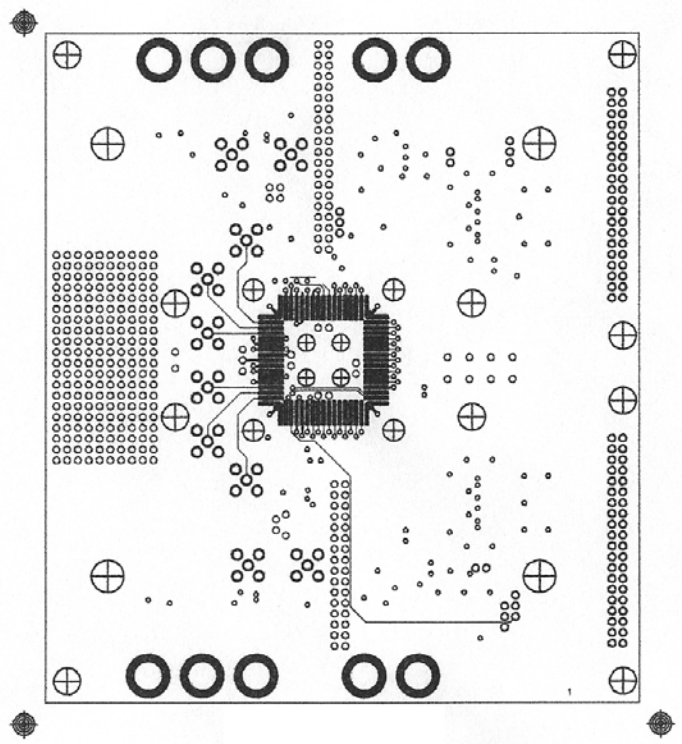


Figure 27. Top Layer Copper

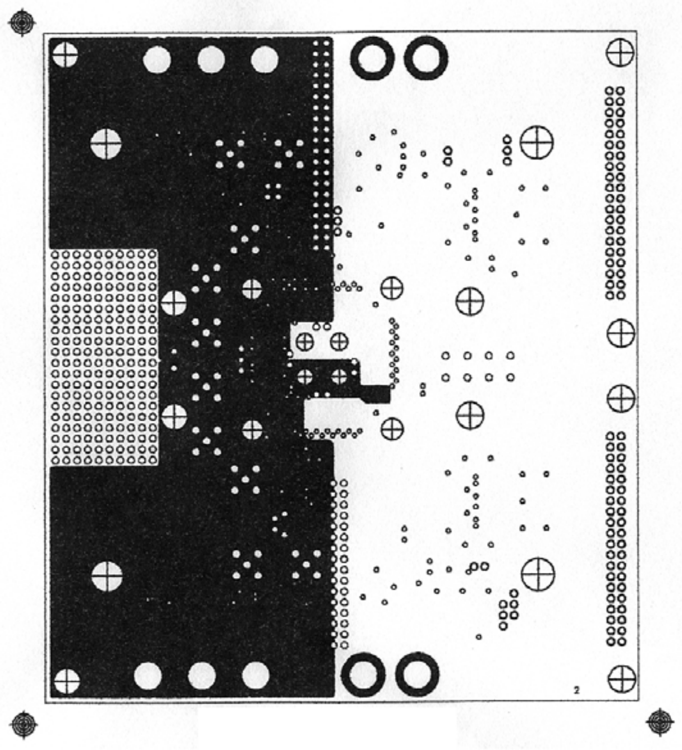


Figure 28. Second Layer Copper

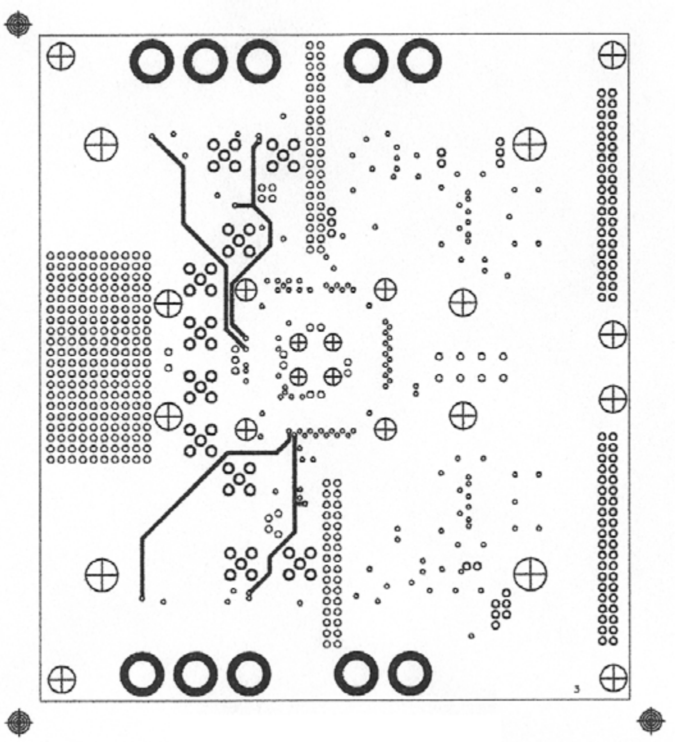


Figure 29. Third Layer Copper

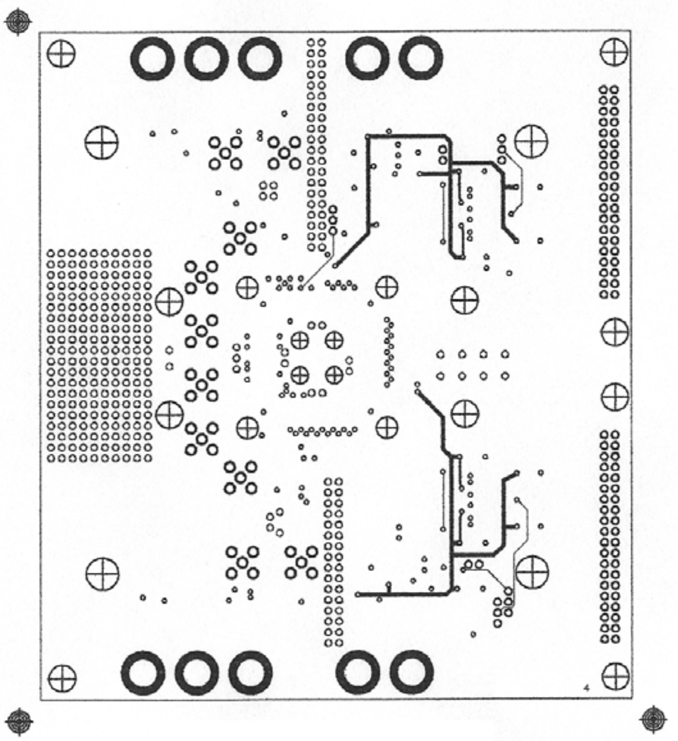


Figure 30. Fourth Layer Copper

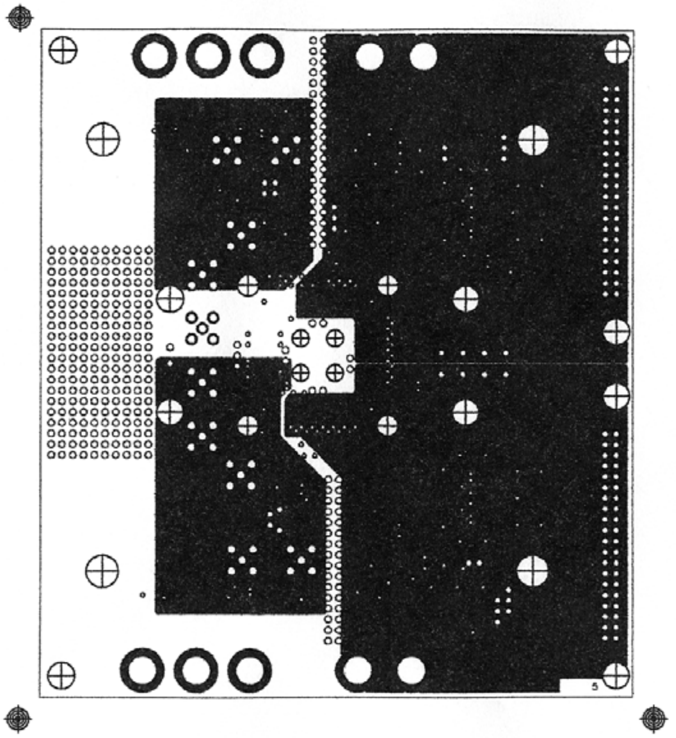


Figure 31. Fifth Layer Copper

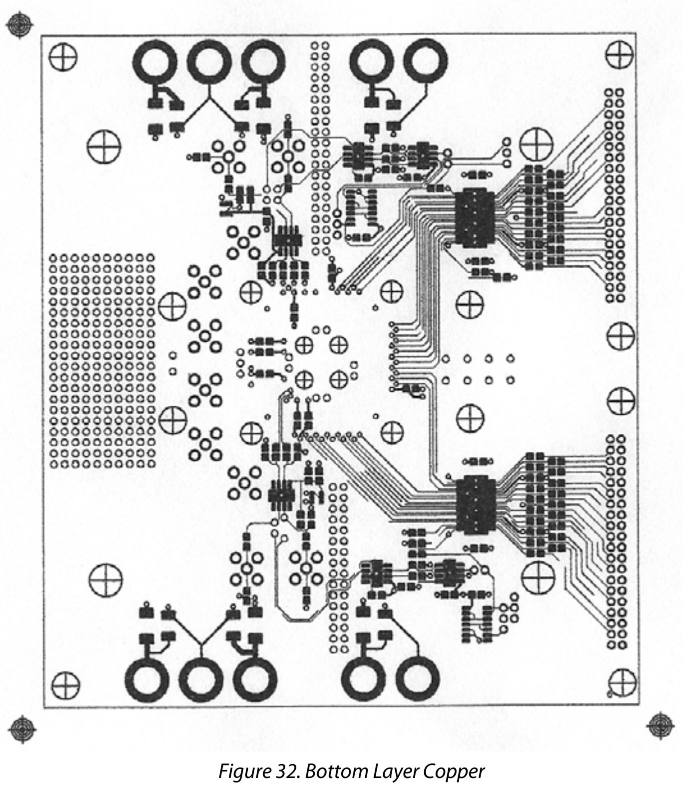


Figure 32. Bottom Layer Copper

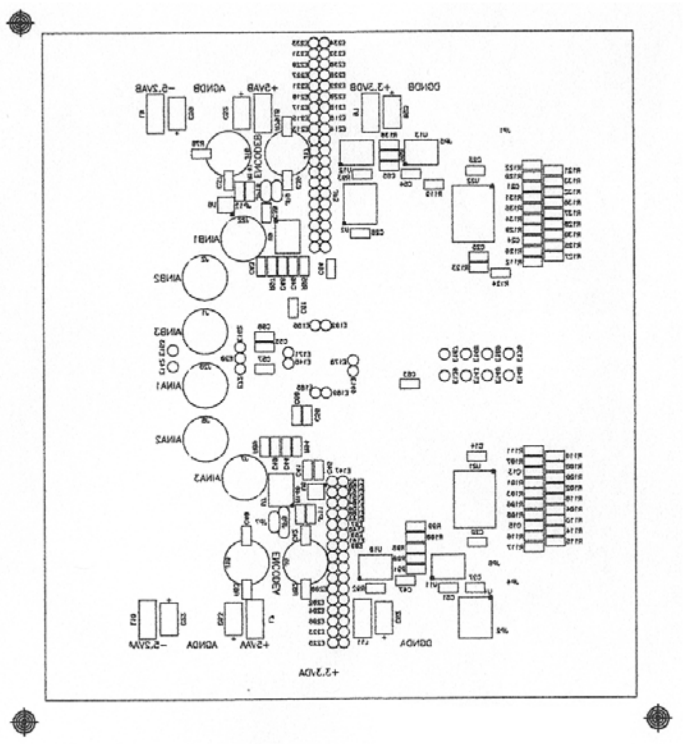


Figure 33. Bottom Silkscreen

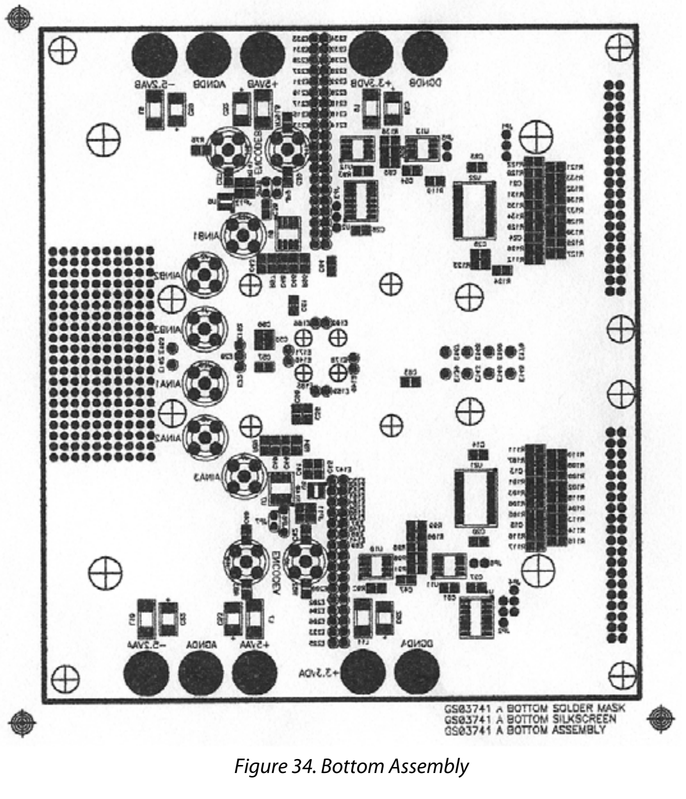
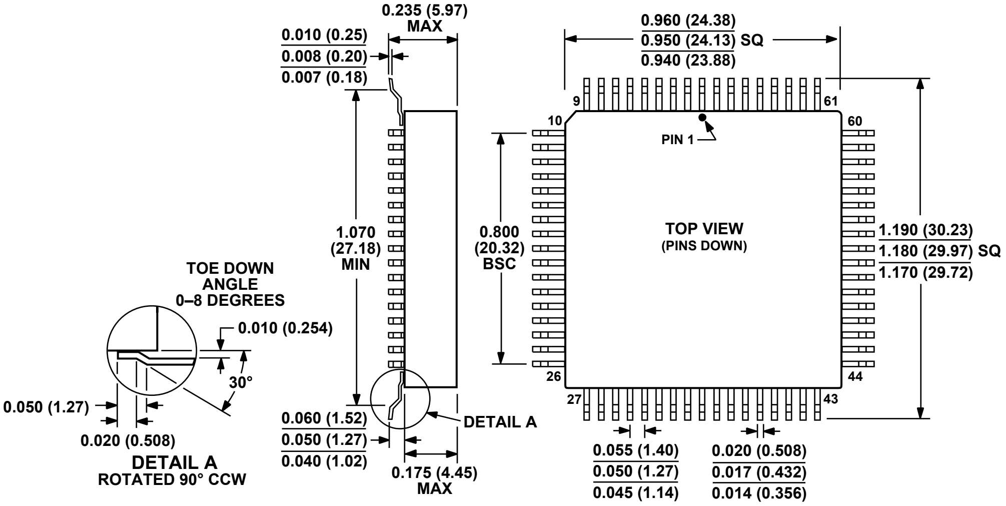


Figure 34. Bottom Assembly

OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 35. 68-Lead Ceramic Leaded Chip Carrier [CLCC]
(Z-68A)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range[1]	Package Description	Package Option
AD10465BZ[2]	−40°C to +85°C	68-Lead Ceramic Leaded Chip Carrier [CLCC]	Z-68A
5962-9961601HXA	−40°C to +85°C	68-Lead Ceramic Leaded Chip Carrier [CLCC]	Z-68A
AD10465/PCB		Evaluation Board with AD10465BZ	

[1] Case temperature.
[2] Z = Pb-free part.