

HiRel FPGAs

Features

- Highly Predictable Performance with 100 Percent Automatic Placement and Routing
- Device Sizes from 1200 to 20,000 gates
- Up to 6, Fast, Low-Skew Clock Networks
- Up to 202 User-Programmable I/O Pins
- More Than 500 Macro Functions
- Up to 1276 Dedicated Flip-Flops
- I/O Drive to 10 mA
- Devices Available to DSCC SMD
- CQFP and CPGA Packaging
- Nonvolatile, User Programmable
- Logic Fully Tested Prior to Shipment

ACT 3 Features

- Highest-Performance, Highest-Capacity FPGA Family
- System Performance to 60 MHz over Military Temperature
- Low-Power 0.8-micron CMOS Technology

3200DX

- 100 MHz System Logic Integration
- Highest Speed FPGA SRAM, up to 2.5 Kbits Configurable Dual-Port SRAM
- Fast Wide-Decode Circuitry

1200XL Features

- Pin for Pin Compatible with ACT 2
- System Performance to 50 MHz over Military Temperature
- Low-Power 0.6-micron CMOS Technology

ACT 2 Features

- Best-Value, High-Capacity FPGA Family
- System Performance to 40 MHz over Military Temperature
- Low-Power 1.0-micron CMOS Technology

ACT 1 Features

- Lowest-Cost FPGA Family
- System Performance to 20 MHz over Military Temperature
- Low-Power 1.0-micron CMOS Technology

Product Family Profile

| Device | Family | ACT 3 | | | 3200DX | | 1200XL |
|--------------------------------------|--------|--------|--------|---------|----------|----------|---------|
| | | A1425A | A1460A | A14100A | A32100DX | A32200DX | A1280XL |
| Capacity | | | | | | | |
| Logic Gates | | 2,500 | 6,000 | 10,000 | 10,000 | 20,000 | 8,000 |
| SRAM Bits | | NA | NA | NA | 2,048 | 2,560 | |
| Logic Modules | | 310 | 848 | 1377 | 1362 | 2414 | 1,232 |
| S-Modules | | 160 | 432 | 697 | 700 | 1230 | 624 |
| C-Modules | | 150 | 416 | 680 | 662 | 1184 | 608 |
| Decode | | NA | NA | NA | 20 | 24 | NA |
| Flip-Flops (maximum) | | 435 | 976 | 1493 | 738 | 1276 | 998 |
| User I/Os (maximum) | | 100 | 168 | 228 | 152 | 202 | 140 |
| Packages ¹ (by pin count) | | | | | | | |
| CPGA | | 133 | 207 | 257 | | | 176 |
| CQFP | | 132 | 196 | 256 | 84 | 208, 256 | 172 |
| Performance | | | | | | | |
| System Speed (maximum) | | 60 MHz | 60 MHz | 60 MHz | 55 MHz | 55 MHz | 50 MHz |

Note:

1. See Product Plan on page 6 for package availability.

Product Family Profile

| Device | Family | ACT 2 | | ACT 1 | |
|--------------------------------------|--------|--------|--------|--------|--------|
| | | A1240A | A1280A | A1010B | A1020B |
| Capacity | | | | | |
| Logic Gates | | 4,000 | 8,000 | 1,200 | 2,000 |
| SRAM Bits | | NA | NA | NA | NA |
| Logic Modules | | 684 | 1232 | 295 | 547 |
| S-Modules | | 348 | 624 | — | — |
| C-Modules | | 336 | 608 | 295 | 547 |
| Decode | | NA | NA | NA | NA |
| Flip-Flops (maximum) | | 568 | 998 | 147 | 273 |
| User I/Os (maximum) | | 104 | 140 | 57 | 69 |
| Packages ¹ (by pin count) | | | | | |
| CPGA | | 132 | 176 | 84 | 84 |
| CQFP | | — | 172 | — | 84 |
| Performance | | | | | |
| System Speed (maximum) | | 40 MHz | 40 MHz | 20 MHz | 20 MHz |

Note:

1. See Product Plan on page 6 for package availability.

High-Reliability, Low-Risk Solution

Actel builds the most reliable field programmable gate arrays (FPGAs) in the industry, with overall antifuse reliability ratings of less than 10 Failures-In-Time (FITs), corresponding to a useful life of more than 40 years. Actel FPGAs have been production proven, with more than five million devices shipped and more than one trillion antifuses manufactured. Actel devices are fully tested prior to shipment, with an outgoing defect level of only 122 ppm. (Further reliability data is available in the “Actel Device Reliability Report.”)

100 Percent Tested

Device functionality is fully tested before shipment and during device programming. Routing tracks, logic modules, and programming, debug, and test circuits are 100 percent tested before shipment. Antifuse integrity also is tested before shipment. Programming algorithms are tested when a device is programmed using Actel’s Activator[®] 2 or Activator 2S programming stations.

Benefits

No Cost Risk—Once you have a Designer/Designer Advantage[™] System, Actel’s CAE software and programming package, you can produce as many chips as you like for just the cost of the device itself, with no NRE charges to eat up your development budget every time you want to try out a new design.

No Time Risk—After entering your design, placement and routing is automatic, and programming the device takes only about 5 to 15 minutes for an average design. You save time in the design entry process by using tools that are familiar to you. The Designer/Designer Advantage System software interfaces with popular CAE packages such as Cadence, Mentor Graphics, OrCAD, and Viewlogic, running on platforms such as HP, Sun, and PC. In addition, synthesis capability is provided with support of synthesis tools from Synopsys, IST, Exemplar, and DATA I/O.

No Reliability Risk—The PLICE[®] antifuse is a one-time programmable, nonvolatile connection. Since Actel devices are permanently programmed, no downloading from EPROM or SRAM storage is required. Inadvertent erasure is impossible, and there is no need to reload the program after power disruptions. Fabrication using a low-power CMOS process means cooler junction temperatures. Actel’s non-PLD architecture delivers lower dynamic operating current. Our reliability tests show a very low failure rate of 66 FITs at 90°C junction temperature with no degradation in AC performance. Special stress testing at wafer test eliminates infant mortalities prior to packaging.

No Security Risk—Reverse engineering of programmed Actel devices from optical or electrical data is extremely difficult. Programmed antifuses cannot be identified from a photograph or by using a SEM. The antifuse map cannot be deciphered either electrically or by microprobing. Each

device has a silicon signature that identifies its origins, down to the wafer lot and fabrication facility.

No Testing Risk—Unprogrammed Actel parts are fully tested at the factory. This includes the logic modules, interconnect tracks, and I/Os. AC performance is ensured by special speed path tests, and programming circuitry is verified on test antifuses. During the programming process, an algorithm is run to ensure that all antifuses are correctly programmed. In addition, Actel's Actionprobe[®] diagnostic tools allow 100 percent observability of all internal nodes to check and debug your design.

Actel FPGA Description

The Actel families of FPGAs offer a variety of packages, speed/performance characteristics, and processing levels for use in all high-reliability and military applications. Devices are implemented in a silicon gate, two-level metal CMOS process, utilizing Actel's PLICE antifuse technology. This unique architecture offers gate array flexibility, high performance, and quick turnaround through user programming. Device utilization is typically 95 percent of available logic modules.

Actel devices also provide system designers with on-chip diagnostic probe/debug capability, allowing the user to observe 100 percent of the nodes within the design, even while the device is operating in-system. All Actel devices include on-chip clock drivers and a hard-wired distribution network.

User-definable I/Os are capable of driving at both TTL and CMOS drive levels. Available packages for the military are the Ceramic Quad Flat Pack (CQFP) and the Ceramic Pin Grid Array (CPGA). See Product Plan on page 6 for details.

All Actel FPGAs are supported by the Actel Designer Series, which offers automatic or user-definable pin assignment, validation of electrical and design rules, automatic placement and routing, timing analysis, user programming, and debug/diagnostic probe capabilities. The Designer Series fully supports schematic capture and backannotated simulation through design kits for Cadence, Mentor Graphics, OrCAD, and Viewlogic. Synthesis is supported with kits for use with synthesis tools from Synopsys, IST, Exemplar, and DATA I/O.

Also available is the ACTmap[™] VHDL optimization and synthesis tool that provides logic synthesis and optimization from PAL language or VHDL description inputs. An FPGA macro generator (ACTgen Macro Builder) is provided, allowing the user easily to create higher-level functions such as counters and adders. Finally, ChipEdit is a graphical/visual design tool that allows the user to modify the automatic place and route results.

ACT 3 Description

The ACT 3 family is the third-generation Actel FPGA family. This family offers the highest-performance and highest-capacity devices, ranging from 2,500 to 10,000 gates, with system performance to 60 MHz over the military temperature range. The devices have four clock distribution networks, including dedicated array and I/O clocks. In addition, the ACT 3 family offers the highest I/O-to-gate ratio available. ACT 3 devices are manufactured using 0.8 micron CMOS technology.

1200XL/3200DX Description

3200DX and 1200XL FPGAs were designed to integrate system logic which is typically implemented in multiple CPLDs, PALs and FPGAs. These devices provide the features and performance required for today's complex, high-speed digital logic systems. The 3200DX family offers the industry's fastest dual-port SRAM for implementing fast FIFOs, LIFOs and temporary data storage.

ACT 2 Description

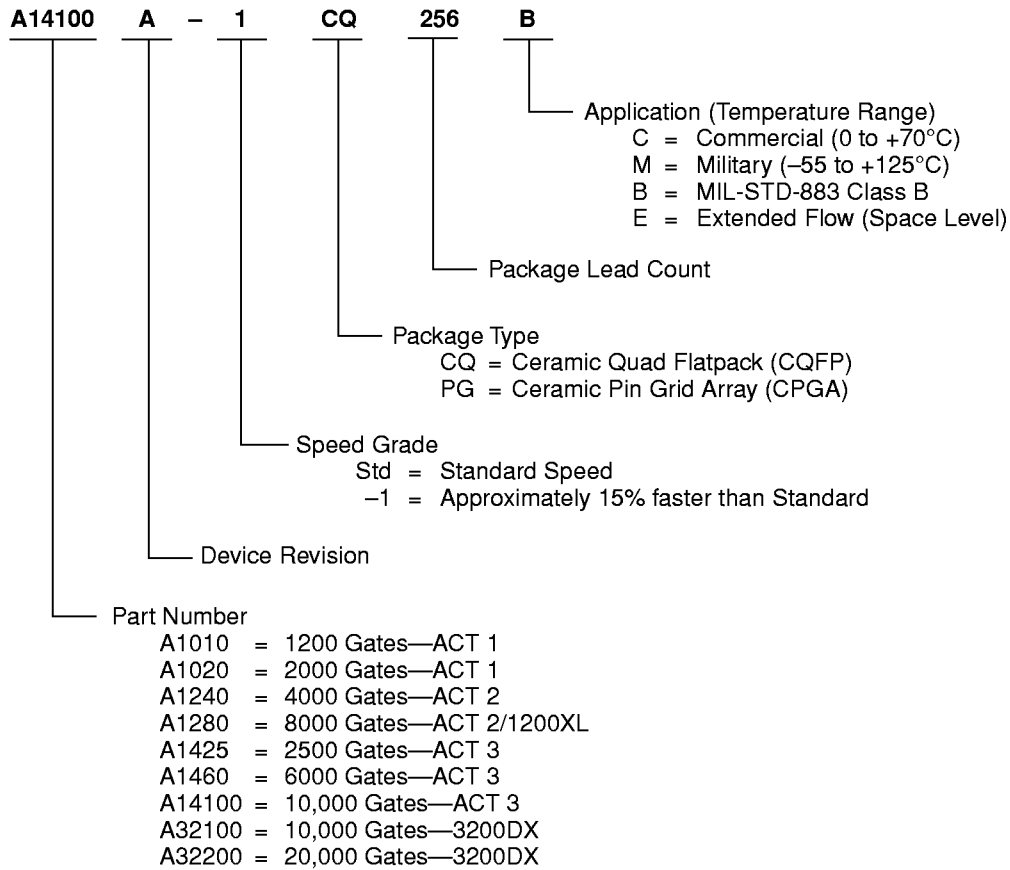
The ACT 2 family is the second-generation Actel FPGA family. This family offers the best-value, high-capacity devices, ranging from 4,000 to 8,000 gates, with system performance to 40 MHz over the military temperature range. The devices have two routed array clock distribution networks. ACT 2 devices are manufactured using 1.0 micron CMOS technology.

ACT 1 Description

The ACT 1 family is the first Actel FPGA family and the first antifuse-based FPGA. This family offers the lowest-cost logic integration, with devices ranging from 1,200 to 2,000 gates, with system performance to 20 MHz over the military temperature range. The devices have one routed array clock distribution network. ACT 1 devices are manufactured using 1.0 micron CMOS technology.



Military Device Ordering Information



DESC SMD/Actel Part Number Cross Reference

| Actel Part Number (Gold Leads) | DSCC SMD (Gold Leads) | DSCC SMD (Solder Dipped) |
|---|----------------------------------|-------------------------------------|
| A1010B-PG84B | 5962-9096403MXC | 5962-9096403MXA |
| A1010B-1PG84B | 5962-9096404MXC | 5962-9096404MXA |
| A1020B-PG84B | 5962-9096503MUC | 5962-9096503MUA |
| A1020B-1PG84B | 5962-9096504MUC | 5962-9096504MUA |
| A1020B-CQ84B | 5962-9096503MTC | 5962-9096503MTA |
| A1020B-1CQ84B | 5962-9096504MTC | 5962-9096504MTA |
| A1240A-PG132B | 5962-9322101MXC | 5962-9322101MXA |
| A1240A-1PG132B | 5962-9322102MXC | 5962-9322102MXA |
| A1280A-PG176B | 5962-9215601MXC | 5962-9215601MXA |
| A1280A-1PG176B | 5962-9215602MXC | 5962-9215602MXA |
| A1280A-CQ172B | 5962-9215601MYC | 5962-9215601MYA |
| A1280A-1CQ172B | 5962-9215602MYC | 5962-9215602MYA |
| A1425A-PG133B | 5962-9552001MXC | 5962-9552001MXA |
| A1425A-1PG133B | 5962-9552002MXC | 5962-9552002MXA |
| A1425A-CQ132B | 5962-9552001MYC | 5962-9552001MYA |
| A1425A-1CQ132B | 5962-9552002MYC | 5962-9552002MYA |
| A1460A-PG207B | 5962-9550801MXC | 5962-9550801MXA |
| A1460A-1PG207B | 5962-9550802MXC | 5962-9550802MXA |
| A1460A-CQ196B | 5962-9550801MYC | 5962-9550801MYA |
| A1460A-1CQ196B | 5962-9550802MYC | 5962-9550802MYA |
| A14100A-PG257B | 5962-9552101MXC | 5962-9552101MXA |
| A14100A-1PG257B | 5962-9552102MXC | 5962-9552102MXA |
| A14100A-CQ256B | 5962-9552101MYC | 5962-9552101MYA |
| A14100A-1CQ256B | 5962-9552102MYC | 5962-9552102MYA |
| A32100DX-CQ84B | TBD | TBD |
| A32100DX-1CQ84B | TBD | TBD |
| A32200DX-CQ208B | TBD | TBD |
| A32200DX-1CQ208B | TBD | TBD |



Product Plan

| | Speed Grade | | Application | | | |
|---------------------------------------|-------------|----|-------------|---|---|---|
| | Std | -1 | C | M | B | E |
| 3200DX Family | | | | | | |
| A32100DX Device | | | | | | |
| 84-pin Ceramic Quad Flatpack (CQFP) | ✓ | ✓ | ✓ | ✓ | ✓ | — |
| A32200DX Device | | | | | | |
| 208-pin Ceramic Quad Flatpack (CQFP) | ✓ | ✓ | ✓ | ✓ | ✓ | — |
| 256-pin Ceramic Quad Flatpack (CQFP) | ✓ | ✓ | ✓ | ✓ | ✓ | — |
| ACT 3 Family | | | | | | |
| A1425A Device | | | | | | |
| 132-pin Ceramic Quad Flatpack (CQFP) | ✓ | ✓ | ✓ | ✓ | ✓ | — |
| 133-pin Ceramic Pin Grid Array (CPGA) | ✓ | ✓ | ✓ | ✓ | ✓ | — |
| A1460A Device | | | | | | |
| 196-pin Ceramic Quad Flatpack (CQFP) | ✓ | ✓ | ✓ | ✓ | ✓ | — |
| 207-pin Ceramic Pin Grid Array (CPGA) | ✓ | ✓ | ✓ | ✓ | ✓ | — |
| A14100A Device | | | | | | |
| 256-pin Ceramic Quad Flatpack (CQFP) | ✓ | ✓ | ✓ | ✓ | ✓ | — |
| 257-pin Ceramic Pin Grid Array (CPGA) | ✓ | ✓ | ✓ | ✓ | ✓ | — |
| 1200XL Family | | | | | | |
| A1280XL Device | | | | | | |
| 172-pin Ceramic Quad Flatpack (CQFP) | ✓ | ✓ | ✓ | ✓ | ✓ | — |
| 176-pin Ceramic Pin Grid Array (CPGA) | ✓ | ✓ | ✓ | ✓ | ✓ | — |
| ACT 2 Family | | | | | | |
| A1240A Device | | | | | | |
| 132-pin Ceramic Pin Grid Array (CPGA) | ✓ | ✓ | ✓ | ✓ | ✓ | — |
| A1280A Device | | | | | | |
| 172-pin Ceramic Quad Flatpack (CQFP) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 176-pin Ceramic Pin Grid Array (CPGA) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| ACT 1 Family | | | | | | |
| A1010B Device | | | | | | |
| 84-pin Ceramic Pin Grid Array (CPGA) | ✓ | ✓ | ✓ | ✓ | ✓ | — |
| A1020B Device | | | | | | |
| 84-pin Ceramic Quad Flatpack (CQFP) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 84-pin Ceramic Pin Grid Array (CPGA) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Applications: C = Commercial Availability: ✓ = Available Now Speed Grade: -1 = Approx. 15% faster than Standard
M = Military P = Planned
B = MIL-STD-883 — = Not Planned
E = Extended Flow

3200DX Device Resources

| FPGA Device Type | Logic Modules | Gate Array Equivalent Gates | User I/Os | | |
|------------------|---------------|-----------------------------|-----------|---------|---------|
| | | | CQFP | | |
| | | | 84-pin | 208-pin | 256-pin |
| A32100DX | 1362 | 10,000 | 60 | — | — |
| A32200DX | 2414 | 20,000 | — | 176 | 202 |

ACT 3 Device Resources

| FPGA Device Type | Logic Modules | Gate Array Equivalent Gates | User I/Os | | | | | |
|------------------|---------------|-----------------------------|-----------|---------|---------|---------|---------|---------|
| | | | CQFP | | | CPGA | | |
| | | | 132-pin | 196-pin | 256-pin | 133-pin | 207-pin | 257-pin |
| A1425A | 310 | 2500 | 100 | — | — | 100 | — | — |
| A1460A | 848 | 6000 | — | 168 | — | — | 168 | — |
| A14100A | 1377 | 10,000 | — | — | 228 | — | — | 228 |

1200XL Device Resources

| FPGA Device Type | Logic Modules | Gate Array Equivalent Gates | User I/Os | |
|------------------|---------------|-----------------------------|-----------|---------|
| | | | CQFP | CPGA |
| | | | 172-pin | 176-pin |
| A1280XL | 1232 | 8000 | 140 | 140 |

ACT 2 Device Resources

| FPGA Device Type | Logic Modules | Gate Array Equivalent Gates | User I/Os | | |
|------------------|---------------|-----------------------------|-----------|---------|---------|
| | | | CQFP | CPGA | |
| | | | 172-pin | 132-pin | 176-pin |
| A1240A | 684 | 4000 | — | 104 | — |
| A1280A | 1232 | 8000 | 140 | — | 140 |

ACT 1 Device Resources

| FPGA Device Type | Logic Modules | Gate Array Equivalent Gates | User I/Os | |
|------------------|---------------|-----------------------------|-----------|--------|
| | | | CQFP | CPGA |
| | | | 84-pin | 84-pin |
| A1010B | 295 | 1200 | — | 57 |
| A1020B | 547 | 2000 | 69 | 69 |

Pin Description

CLK Clock (Input)
ACT 1 only. TTL Clock input for global clock distribution network. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKA Clock A (Input)
ACT 3, 1200XL, and ACT 2 only. TTL Clock input for global clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB Clock B (Input)

ACT 3, 1200XL, and ACT 2 only. TTL Clock input for global clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-wired) Array Clock (Input)

ACT 3 only. TTL Clock input for sequential modules. This input is directly wired to each S-module and offers clock speeds independent of the number of S-modules being driven. This pin can also be used as an I/O.

I/O Input/Output (Input, Output)

I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW.

IOCLK Dedicated (Hard-wired) I/O Clock (Input)

ACT 3 only. TTL Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

IOPCL Dedicated (Hard-wired) I/O Preset/Clear (Input)

ACT 3 only. TTL input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

MODE Mode (Input)

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. When the MODE pin is LOW, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled high when required.

NC No Connection

This pin is not connected to circuitry within the device.

PRA/I/O Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB/I/O Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} 5V Supply Voltage

HIGH supply voltage.

QCLKA/B,C,D Quadrant Clock (Input/Output)

These four pins are the quadrant clock inputs. When not used as a register control signal, these pins can function as general purpose I/O.

TCK Test Clock

Clock signal to shift the JTAG data into the device. This pin functions as an I/O when the JTAG fuse is not programmed.

TDI Test Data In

Serial data input for JTAG instructions and data. Data is shifted in on the rising edge of TCLK. This pin functions as an I/O when the JTAG fuse is not programmed.

TDO Test Data Out

Serial data output for JTAG instructions and test data. This pin functions as an I/O when the JTAG fuse is not programmed.

TMS Test Mode Select

Serial data input for JTAG test mode. Data is shifted in on the rising edge of TCLK. This pin functions as an I/O when the JTAG fuse is not programmed.

Actel MIL-STD-883 Product Flow

| Step | Screen | 833 Method | 833—Class B Requirement |
|------|--|--|-------------------------|
| 1.0 | Internal Visual | 2010, Test Condition B | 100% |
| 2.0 | Temperature Cycling | 1010, Test Condition C | 100% |
| 3.0 | Constant Acceleration | 2001, Test Condition E (min), Y1, Orientation Only | 100% |
| 4.0 | Seal a.Fine b.Gross | 1014 | 100% 100% |
| 5.0 | Visual Inspection | 2009 | 100% |
| 6.0 | Pre-burn-in Electrical Parameters | In accordance with Actel applicable device specification | 100% |
| 7.0 | Burn-in Test | 1015 Condition D 160 hours @ 125°C Min. | 100% |
| 8.0 | Interim (Post-burn-in) Electrical Parameters | In accordance with Actel applicable device specification | 100% |
| 9.0 | Percent Defective Allowable | 5% | All Lots |
| 10.0 | Final Electrical Test | In accordance with Actel applicable device specification | |
| | a. Static Tests | | 100% |
| | (1) 25°C (Subgroup 1, Table I, 5005) | | |
| | (2) -55°C and +125°C (Subgroups 2, 3, Table I, 5005) | | |
| | b. Dynamic and Functional Tests | | 100% |
| | (1) 25°C (Subgroup 7, Table I, 5005) | | |
| | (2) -55°C and +125°C (Subgroups 8A and 8B, Table I, 5005) | | |
| | c. Switching Tests at 25°C (Subgroup 9, Table I, 5005) | | 100% |
| 11.0 | Qualification or Quality Confirmation Inspection Test Sample Selection (Group A and Group B) | 5005 | All Lots |
| 12.0 | External Visual | 2009 | 100% |

Actel Extended Flow^{1, 2}

| Screen | Method | Requirement |
|---|--|-------------------|
| 1. Wafer Lot Acceptance ³ | 5007 with step coverage waiver | All Lots |
| 2. Destructive In-Line Bond Pull ⁴ | 2011, condition D | Sample |
| 3. Internal Visual | 2010, condition A | 100% |
| 4. Serialization | | 100% |
| 5. Temperature Cycling | 1010, condition C | 100% |
| 6. Constant Acceleration | 2001, condition E (min), Y ₁ orientation only | 100% |
| 7. Visual Inspection | 2009 | 100% |
| 8. Particle Impact Noise Detection | 2020, condition A | 100% |
| 9. Radiographic | 2012 | 100% |
| 10. Pre-burn-in Test | In accordance with Actel applicable device specification | 100% |
| 11. Burn-in Test | 1015, condition D, 240 hours @ 125°C minimum | 100% |
| 12. Interim (Post-burn-in) Electrical Parameters | In accordance with Actel applicable device specification | 100% |
| 13. Reverse Bias Burn-in | 1015, condition C, 72 hours @ 150°C minimum | 100% |
| 14. Interim (Post-burn-in) Electrical Parameters | In accordance with Actel applicable device specification | 100% |
| 15. Percent Defective Allowable (PDA) Calculation | 5%, 3% functional parameters @ 25°C | All Lots |
| 16. Final Electrical Test | In accordance with Actel applicable device specification | 100% |
| a. Static Tests | | 100% |
| (1) 25°C (Subgroup 1, Table1) | 5005 | |
| (2) -55°C and +125°C (Subgroups 2, 3, Table 1) | 5005 | |
| b. Dynamic and Functional Tests | | 100% |
| (1) 25°C (Subgroup 7, Table 15) | 5005 | |
| (2) -55°C and +125°C (Subgroups 5 and 6, 8a and b, Table 1) | 5005 | |
| c. Switching Tests at 25°C (Subgroup 9, Table 1, 5005) | 5005 | 100% |
| 17. Seal | 1014 | 100% |
| a. Fine | | |
| b. Gross | | |
| 18. Qualification or Quality Conformance Inspection Test Sample Selection | 5005 | Group A & Group B |
| 19. External Visual | 2009 | 100% |

Notes:

- Actel offers the Extended Flow in order to satisfy those customers that require additional screening beyond the requirements of MIL-STD-883, Class B. Actel is compliant to the requirements of MIL-STD-883, Paragraph 1.2.1, and MIL-I-38535, Appendix A. Actel is offering this extended flow incorporating the majority of the screening procedures as outlined in Method 5004 of MIL-STD-883 Class S. The exceptions to Method 5004 are shown in notes 2 to 4 below.
- Method 5004 requires a 100 percent Radiation latch-up testing to Method 1020. Actel will not be performing any radiation testing, and this requirement must be waived in its entirety.
- Wafer lot acceptance is performed to Method 5007; however the step coverage requirement as specified in Method 2018 must be waived.
- Method 5004 requires a 100 percent, nondestructive bond pull to Method 2023. Actel substitutes a destructive bond pull to Method 2011, condition D on a sample basis only.

Absolute Maximum Ratings¹

Free air temperature range

| Symbol | Parameter | Limits | Units |
|------------------|--------------------------------------|-------------------------------|-------|
| V _{CC} | DC Supply Voltage ^{2, 3, 4} | -0.5 to +7.0 | V |
| V _I | Input Voltage | -0.5 to V _{CC} + 0.5 | V |
| V _O | Output Voltage | -0.5 to V _{CC} + 0.5 | V |
| I _{IO} | I/O Source Sink Current ⁵ | ±20 | mA |
| T _{STG} | Storage Temperature | -65 to +150 | °C |

Notes:

- Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.
- Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 V or less than GND - 0.5 V, the internal protection diode will be forward biased and can draw excessive current.

Recommended Operating Conditions

| Parameter | Commercial | Military | Units |
|--------------------------------|------------|-------------|------------------|
| Temperature Range ¹ | 0 to +70 | -55 to +125 | °C |
| Power Supply Tolerance | ±5 | ±10 | %V _{CC} |

Note:

- Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc} , and the junction to ambient air characteristic is θ_{ja} . The thermal characteristics for θ_{ja} are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CPGA 176-pin package at military temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. military temp.}}{\theta_{ja} \text{ (°C/W)}} = \frac{150^\circ\text{C} - 125^\circ\text{C}}{23^\circ\text{C/W}} = 1.1 \text{ W}$$

| Package Type | Pin Count | θ_{jc} | θ_{ja} Still Air | θ_{ja} 300 ft/min | Units |
|------------------------|-----------|---------------|----------------------------|-----------------------------|-------|
| Ceramic Pin Grid Array | 84 | 20 | 33 | 20 | °C/W |
| | 132 | 20 | 26 | 16 | °C/W |
| | 133 | 20 | 37 | 24 | °C/W |
| | 176 | 20 | 23 | 12 | °C/W |
| | 207 | 20 | 22 | 14 | °C/W |
| | 257 | 20 | 21 | 13 | °C/W |
| Ceramic Quad Flatpack | 84 | 13 | 40 | 25 | °C/W |
| | 132 | 13 | 55 | 30 | °C/W |
| | 172 | 13 | 25 | 15 | °C/W |
| | 196 | 13 | 36 | 24 | °C/W |
| | 256 | 13 | 30 | 18 | °C/W |

Electrical Specifications

| Symbol | Parameter | Test Condition | Commercial | | Military | | Units |
|----------------|---------------------------------|---|------------|----------------|----------|----------------|---------------|
| | | | Min. | Max. | Min. | Max. | |
| $V_{OH}^{1,2}$ | HIGH Level Output | $I_{OH} = -4 \text{ mA (CMOS)}$ | | | 3.7 | | V |
| | | $I_{OH} = -6 \text{ mA (CMOS)}$ | 3.84 | | | | V |
| $V_{OL}^{1,2}$ | LOW Level Output | $I_{OL} = +6 \text{ mA (CMOS)}$ | | 0.33 | | 0.4 | V |
| V_{IH} | HIGH Level Input | TTL Inputs | 2.0 | $V_{CC} + 0.3$ | 2.0 | $V_{CC} + 0.3$ | V |
| V_{IL} | LOW Level Input | TTL Inputs | -0.3 | 0.8 | -0.3 | 0.8 | V |
| I_{IN} | Input Leakage | $V_I = V_{CC}$ or GND | -10 | +10 | -10 | +10 | μA |
| I_{OZ} | 3-state Output Leakage | $V_O = V_{CC}$ or GND | -10 | +10 | -10 | +10 | μA |
| C_{IO} | I/O Capacitance ^{3,4} | | | 10 | | 10 | pF |
| $I_{CC(S)}$ | Standby V_{CC} Supply Current | $V_I = V_{CC}$ or GND, $I_O = 0 \text{ mA}$ | | | | | |
| | | ACT 1 | | 3 | | 20 | mA |
| | | ACT 2/3/1200XL/3200DX | | 2 | | 20 | mA |
| $I_{CC(D)}$ | Dynamic V_{CC} Supply Current | See "Power Dissipation" Section | | | | | |

Notes:

1. Actel devices can drive and receive either CMOS or TTL signal levels. No assignment of I/Os as TTL or CMOS is required.
2. Tested one output at a time, $V_{CC} = \text{min.}$
3. Not tested; for information only.
4. $V_{OUT} = 0V$, $f = 1 \text{ MHz}$

General Power Equation

$$P = [I_{CC\text{standby}} + I_{CC\text{active}}] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M$$

Where:

$I_{CC\text{standby}}$ is the current flowing when no inputs or outputs are changing.

$I_{CC\text{active}}$ is the current flowing due to CMOS switching.

I_{OL} , I_{OH} are TTL sink/source currents.

V_{OL} , V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL} .

M equals the number of outputs driving TTL loads to V_{OH} .

An accurate determination of N and M is problematical because their values depend on the family type, on design details, and on the system I/O. The power can be divided into two components—static and active.

Static Power Component

Actel FPGAs have small static power components that result in power dissipation lower than that of PALs or PLDs. By integrating multiple PALs or PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated below for commercial, worst-case conditions.

| Family | I_{CC} | V_{CC} | Power |
|---------------|----------|----------|---------|
| ACT 1 | 3 mA | 5.25 V | 15.8 mW |
| 1200XL/3200DX | 2 mA | 5.25V | 10.5mW |
| ACT 2 | 2 mA | 5.25 V | 10.5 mW |
| ACT 3 | 2 mA | 5.25 V | 10.5 mW |

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that

can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by the Equation 1

$$\text{Power (}\mu\text{W)} = C_{EQ} * V_{CC}^2 * F \quad (1)$$

where:

C_{EQ} is the equivalent capacitance expressed in pF.

V_{CC} is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring I_{CC} active at a specified frequency and voltage for each circuit component of interest. Measurements are made over a range of frequencies at a fixed value of V_{CC} . Equivalent capacitance is frequency independent so that the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

C_{EQ} Values for Actel FPGAs

| | 1200XL | | | |
|--|--------|--------|-------|-------|
| | ACT 1 | 3200DX | ACT 2 | ACT 3 |
| Modules (C_{EQM}) | 3.7 | 5.2 | 5.8 | 6.7 |
| Input Buffers (C_{EQI}) | 22.1 | 11.6 | 12.9 | 7.2 |
| Output Buffers (C_{EQO}) | 31.2 | 23.8 | 23.8 | 10.4 |
| Routed Array Clock Buffer Loads (C_{EQCR}) | 4.6 | 3.5 | 3.9 | 1.6 |
| Dedicated Clock Buffer Loads (C_{EQCD}) | n/a | n/a | n/a | 0.7 |
| I/O Clock Buffer Loads (C_{EQCI}) | n/a | n/a | n/a | 0.9 |

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 2 shows a piecewise linear summation over all components, it applies to all ACT 1, 1200XL, ACT 2, and ACT 3 devices. Since the ACT 1 family has only one routed array clock, the terms labeled routed_Clk2, dedicated_Clk, and IO_Clk do not apply. Similarly, the ACT 2 family has two routed array clocks, and the dedicated_Clk and IO_Clk terms do not apply. For ACT 3 devices, all terms will apply.

$$\text{Power} = V_{CC}^2 * [(m * C_{EQM} * f_m)_{\text{modules}} + (n * C_{EQI} * f_n)_{\text{inputs}} + (p * (C_{EQO} + C_L) * f_p)_{\text{outputs}} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{\text{routed_Clk1}} + (r_1 * f_{q1})_{\text{routed_Clk1}} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{\text{routed_Clk2}} + (r_2 * f_{q2})_{\text{routed_Clk2}} + 0.5 * (s_1 * C_{EQCD} * f_{s1})_{\text{dedicated_Clk}} + (s_2 * C_{EQCI} * f_{s2})_{\text{IO_Clk}}] \quad (2)$$

where:

- m = Number of logic modules switching at f_m
- n = Number of input buffers switching at f_n
- p = Number of output buffers switching at f_p
- q_1 = Number of clock loads on the first routed array clock (all families)
- q_2 = Number of clock loads on the second routed array clock (ACT 2, 1200XL, ACT 3 only)
- r_1 = Fixed capacitance due to first routed array clock (all families)
- r_2 = Fixed capacitance due to second routed array clock (ACT 2, 1200XL, ACT 3 only)
- s_1 = Fixed number of clock loads on the dedicated array clock (ACT 3 only)
- s_2 = Fixed number of clock loads on the dedicated I/O clock (ACT 3 only)
- C_{EQM} = Equivalent capacitance of logic modules in pF
- C_{EQI} = Equivalent capacitance of input buffers in pF
- C_{EQO} = Equivalent capacitance of output buffers in pF
- C_{EQCR} = Equivalent capacitance of routed array clock in pF
- C_{EQCD} = Equivalent capacitance of dedicated array clock in pF
- C_{EQCI} = Equivalent capacitance of dedicated I/O clock in pF
- C_L = Output lead capacitance in pF
- f_m = Average logic module switching rate in MHz
- f_n = Average input buffer switching rate in MHz
- f_p = Average output buffer switching rate in MHz
- f_{q1} = Average first routed array clock rate in MHz (all families)
- f_{q2} = Average second routed array clock rate in MHz (ACT 2, 1200XL, ACT 3 only)
- f_{s1} = Average dedicated array clock rate in MHz (ACT 3 only)
- f_{s2} = Average dedicated I/O clock rate in MHz (ACT 3 only)

Fixed Capacitance Values for Actel FPGAs (pF)

| Device Type | r ₁ routed_Clk1 | r ₂ routed_Clk2 |
|-------------|-------------------------------|-------------------------------|
| A1010B | 41 | n/a |
| A1020B | 69 | n/a |
| A1240A | 134 | 134 |
| A1280A | 168 | 168 |
| A1280XL | 168 | 168 |
| A1425A | 75 | 75 |
| A1460A | 165 | 165 |
| A14100A | 195 | 195 |
| A32100DX | 178 | 178 |
| A32200DX | 230 | 230 |

Fixed Clock Loads (s₁/s₂—ACT 3 Only)

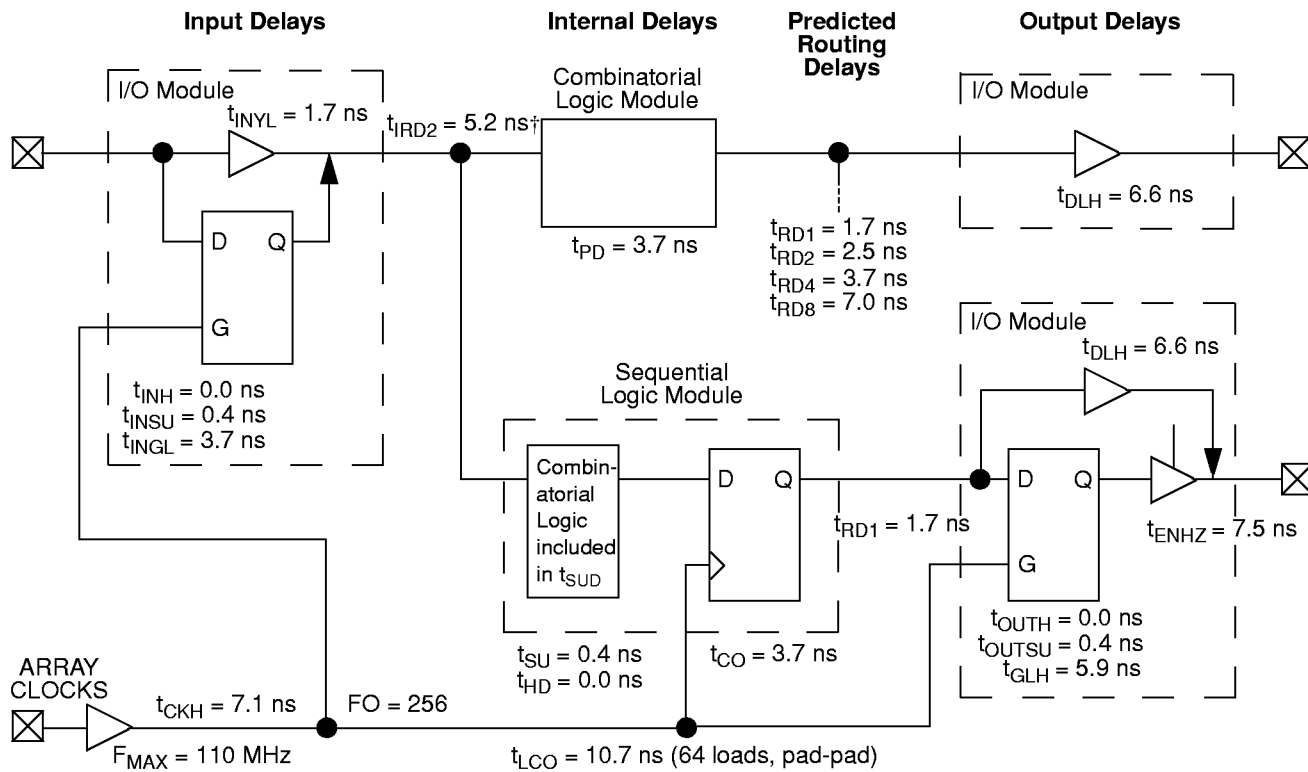
| Device Type | s ₁ Clock Loads on Dedicated Array Clock | s ₂ Clock Loads on Dedicated I/O Clock |
|-------------|--|--|
| A1425A | 160 | 100 |
| A1460A | 432 | 168 |
| A14100A | 697 | 228 |

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data values input to the circuit. The guidelines in the table below are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation.

| Type | ACT 1 | ACT 2/1200XL/3200DX | ACT 3 |
|---|----------------|---------------------------|---------------------------|
| Logic modules (m) | 90% of modules | 80% of modules | 80% of modules |
| Input switching (n) | # inputs/4 | # inputs/4 | # inputs/4 |
| Outputs switching (p) | #outputs/4 | #outputs/4 | #outputs/4 |
| First routed array clock loads (q ₁) | 40% of modules | 40% of sequential modules | 40% of sequential modules |
| Second routed array clock loads (q ₂) | n/a | 40% of sequential modules | 40% of sequential modules |
| Load capacitance (C _L) | 35 pF | 35 pF | 35 pF |
| Average logic module switching rate (f _m) | F/10 | F/10 | F/10 |
| Average input switching rate (f _n) | F/5 | F/5 | F/5 |
| Average output switching rate (f _p) | F/10 | F/10 | F/10 |
| Average first routed array clock rate (f _{q1}) | F | F | F/2 |
| Average second routed array clock rate (f _{q2}) | n/a | F/2 | F/2 |
| Average dedicated array clock rate (f _{s1}) | n/a | n/a | F |
| Average dedicated I/O clock rate (f _{s2}) | n/a | n/a | F |

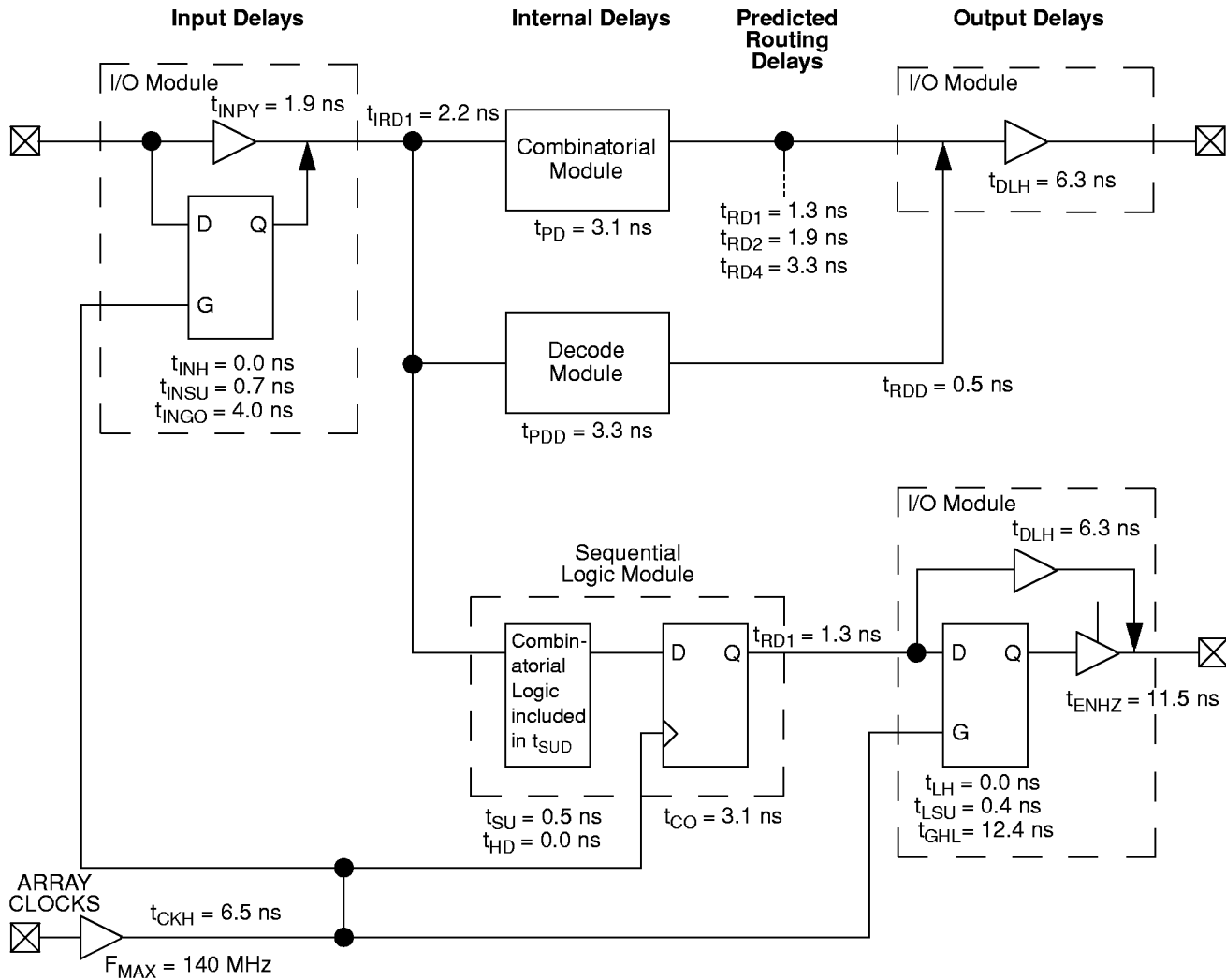
1200XL Timing Model*



*Values shown for A1280XL-1 at worst-case military conditions.

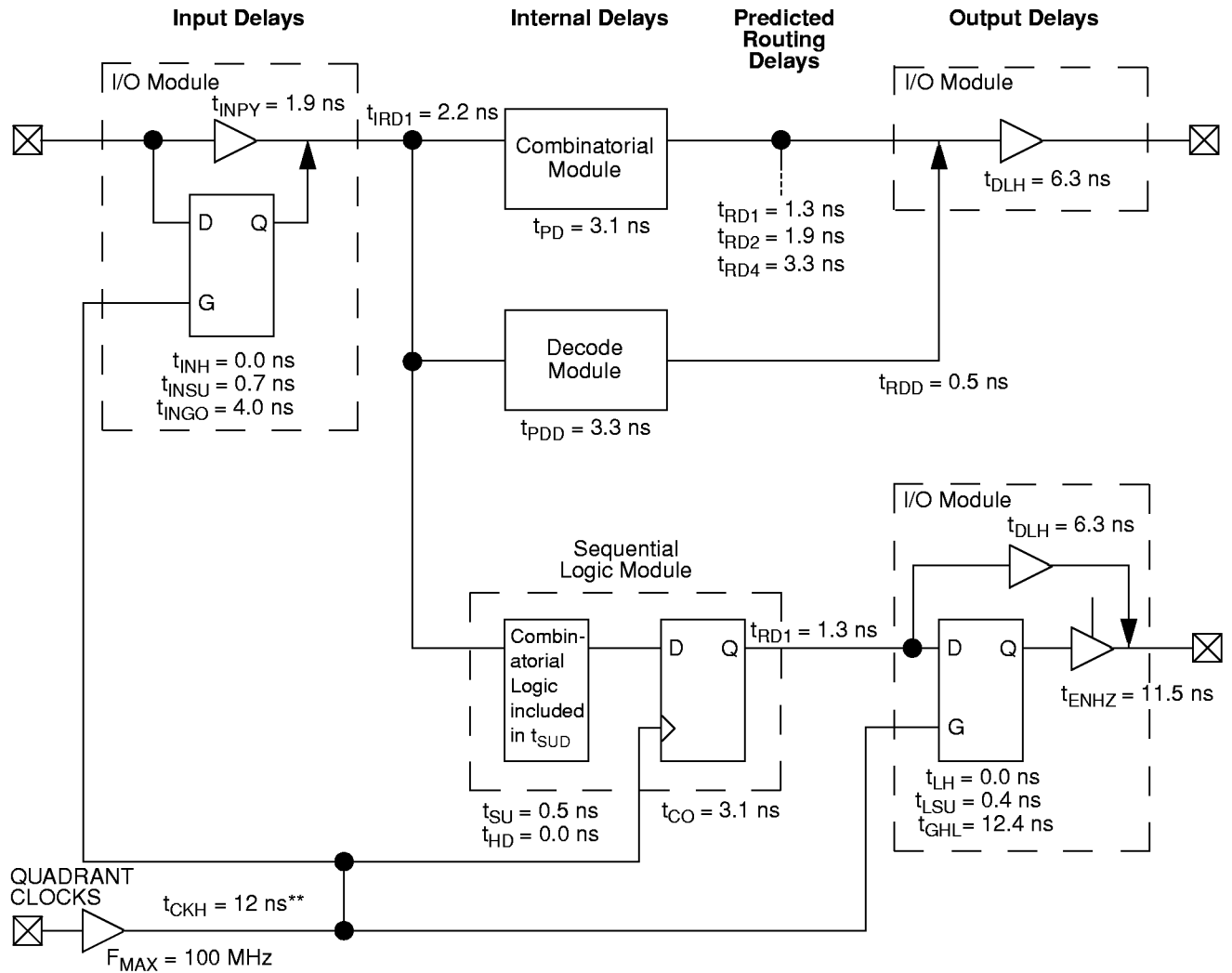
† Input Module Predicted Routing Delay

3200DX Timing Model (Logic Functions using Array Clocks)*



*Values shown for A32100DX-1 at worst-case military conditions.

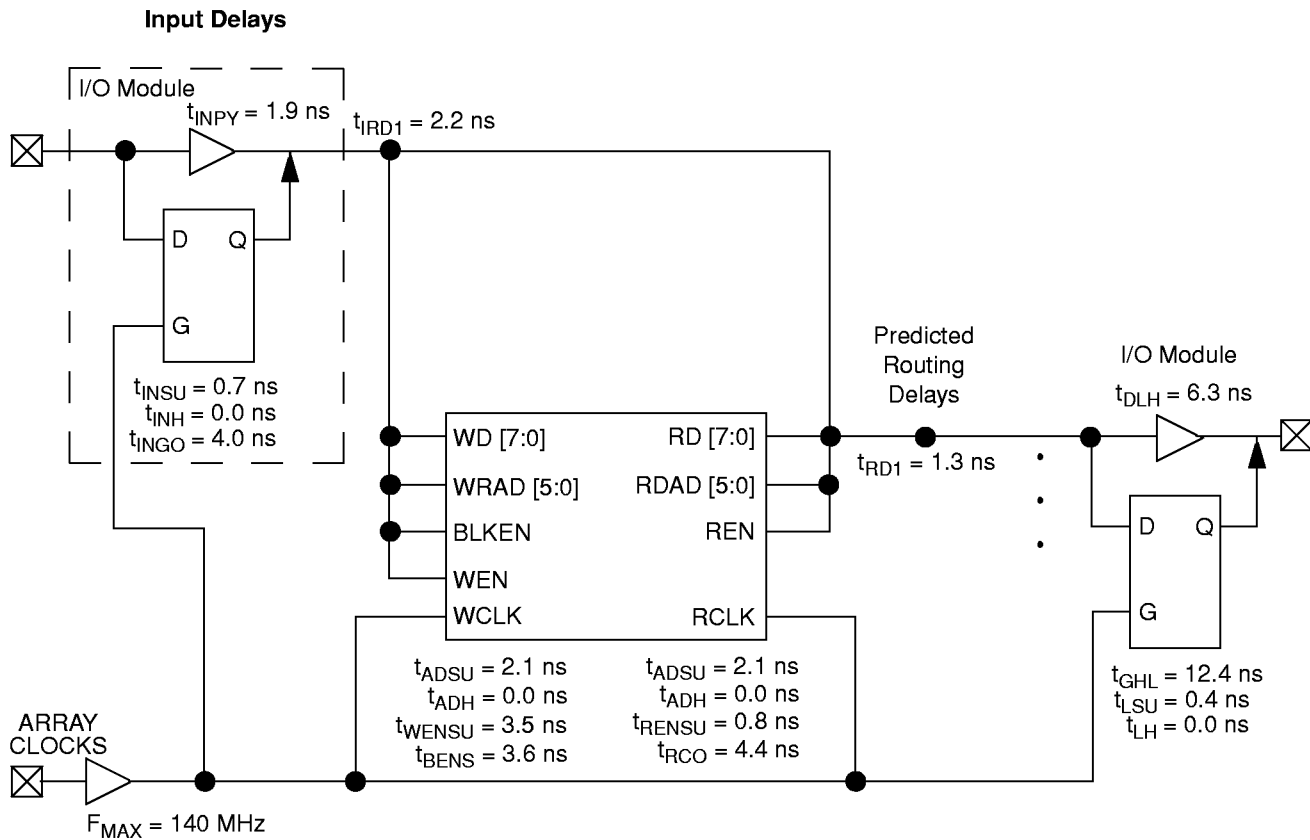
3200DX Timing Model (Logic Functions using Quadrant Clocks)*



* Values shown for A32100DX-1 at worst-case military conditions.

** Load dependent.

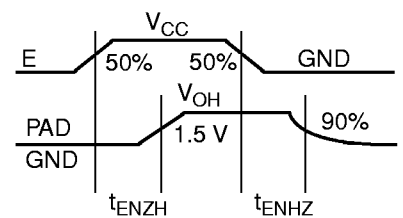
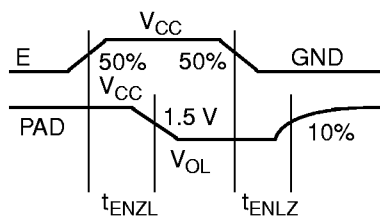
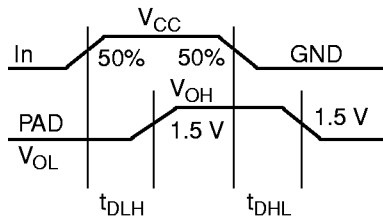
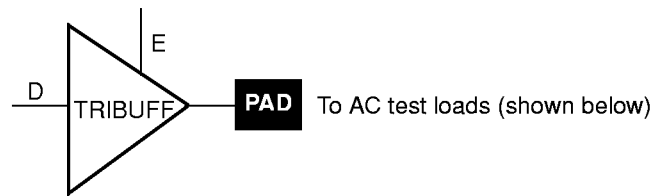
3200DX Timing Model (SRAM Functions)*



*Values shown for A32100DX-1 at worst-case military conditions.

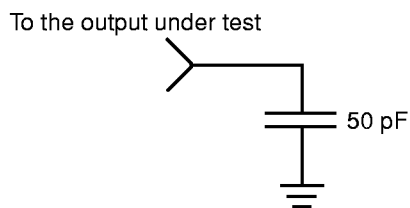
Parameter Measurement

Output Buffer Delays

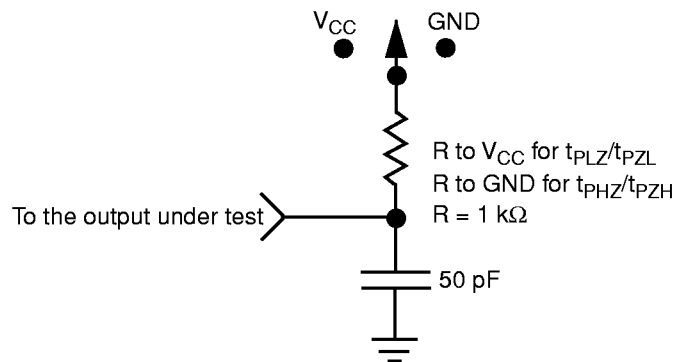


AC Test Load

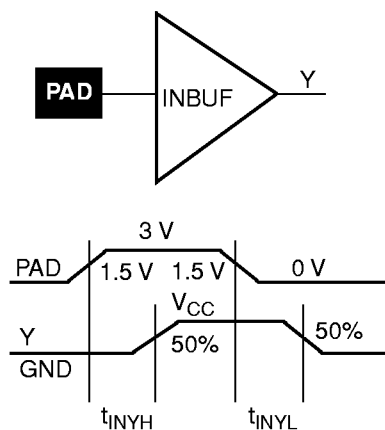
Load 1
(Used to measure propagation delay)



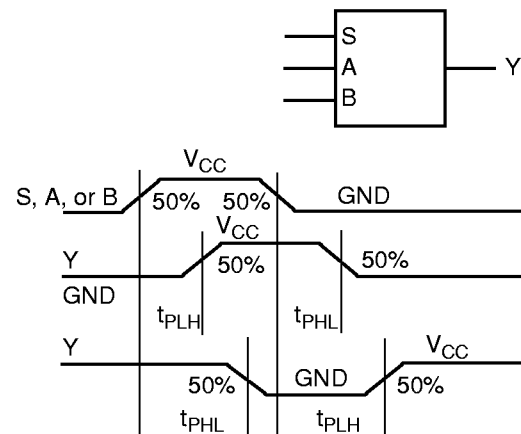
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

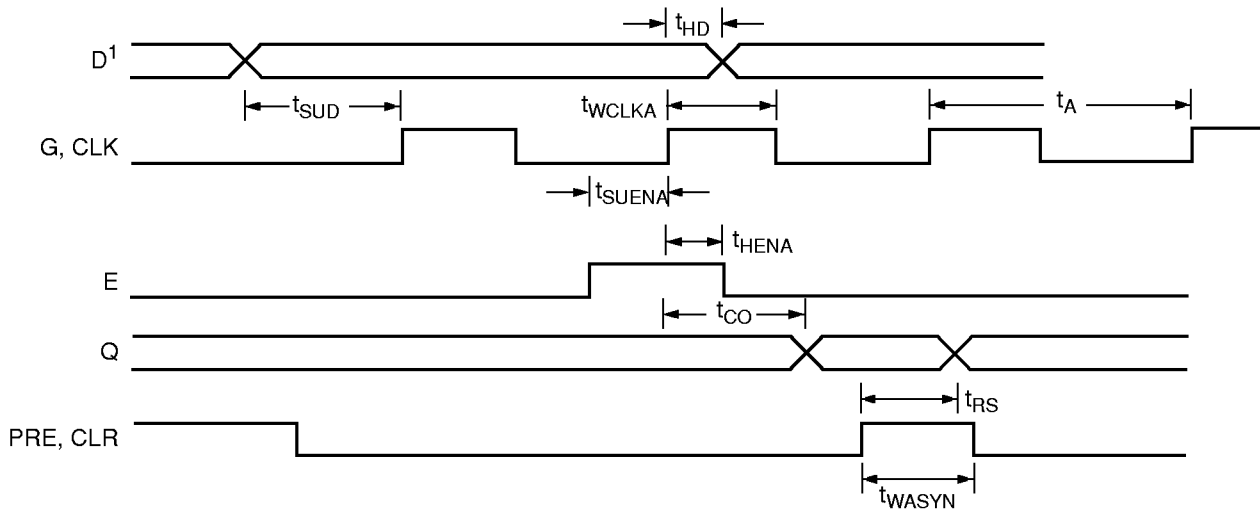
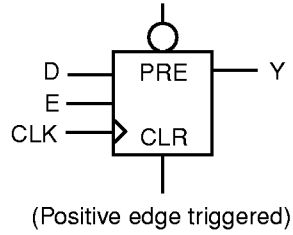


Combinatorial Macro Delays



Sequential Timing Characteristics

Flip-Flops and Latches (ACT 1, ACT 2, and 1200XL/3200DX)

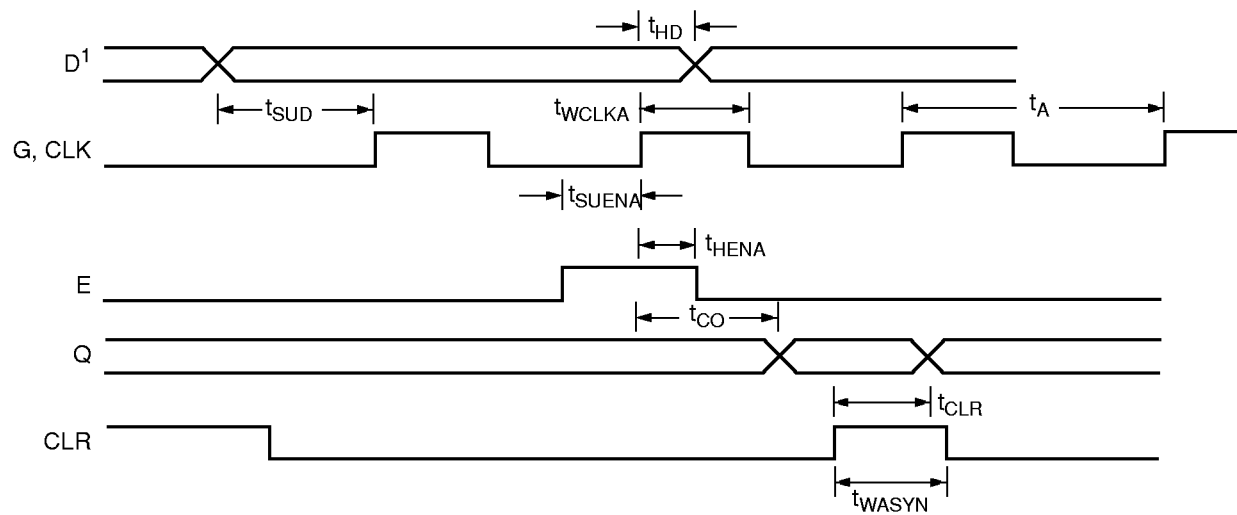
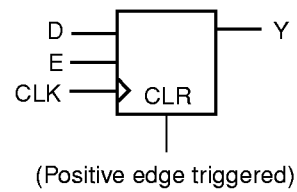


Note:

1. D represents all data functions involving A , B , and S for multiplexed flip-flops.

Sequential Timing Characteristics (continued)

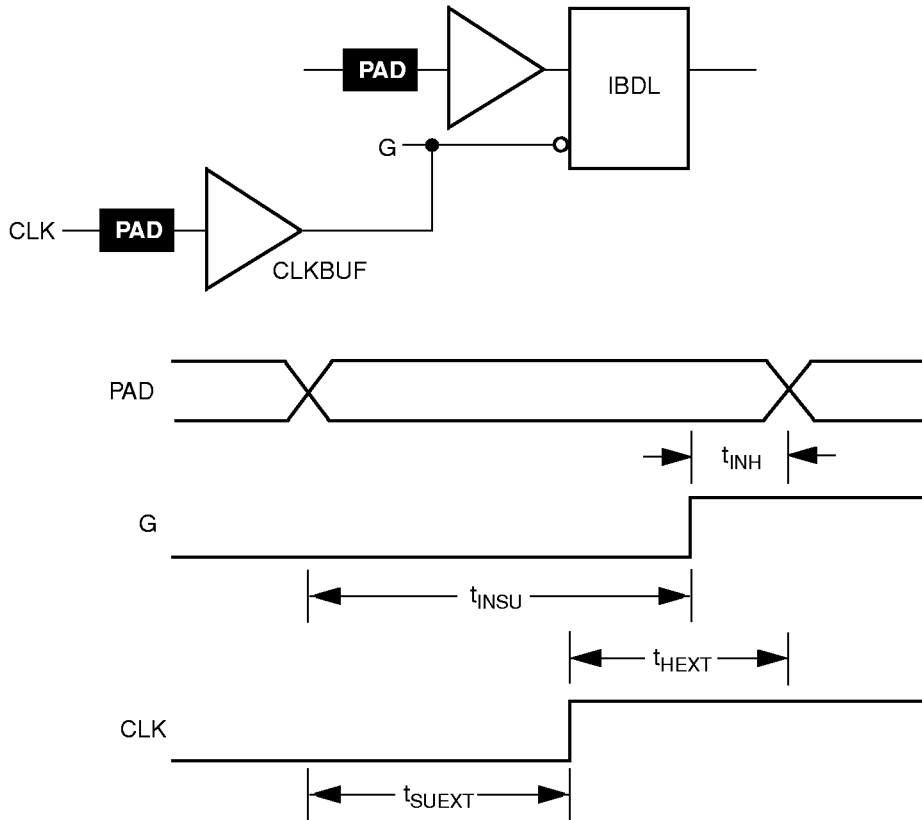
Flip-Flops and Latches (ACT 3)

**Note:**

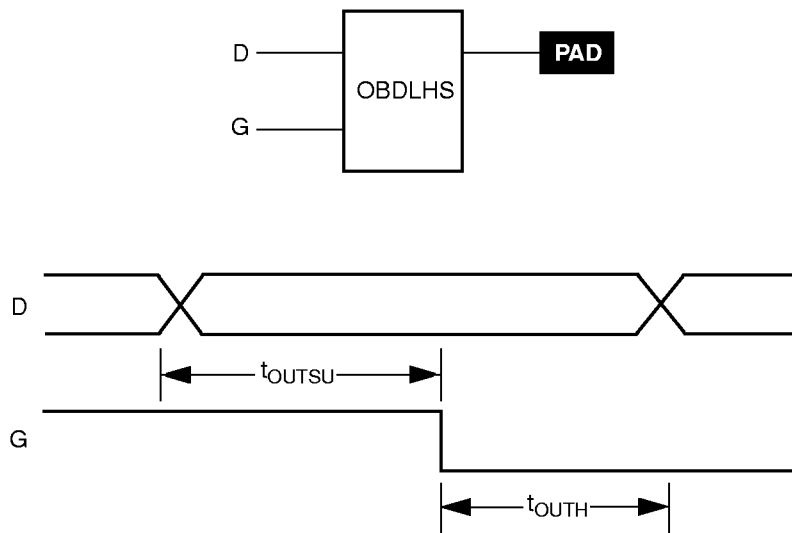
1. D represents all data functions involving A, B, and S for multiplexed flip-flops.

Sequential Timing Characteristics (continued)

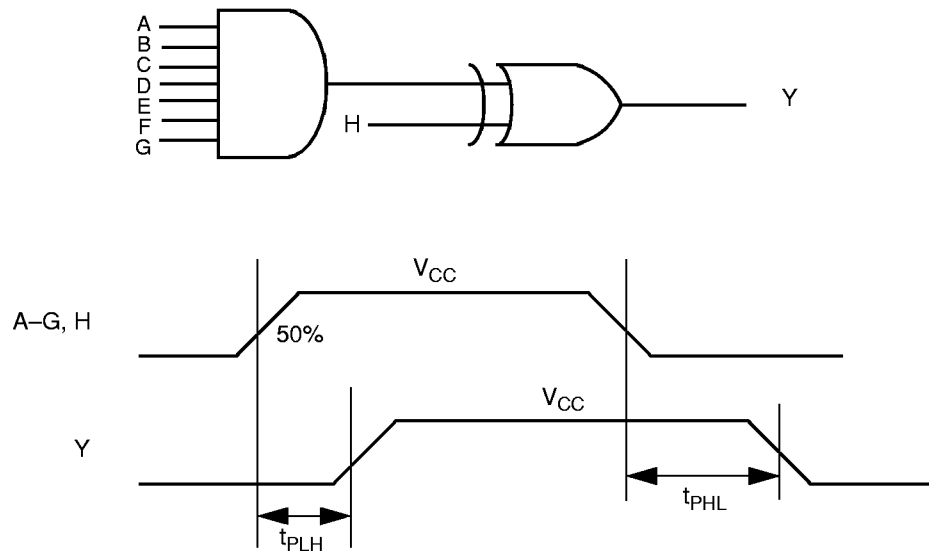
Input Buffer Latches (ACT 2 and 1200XL/3200DX)



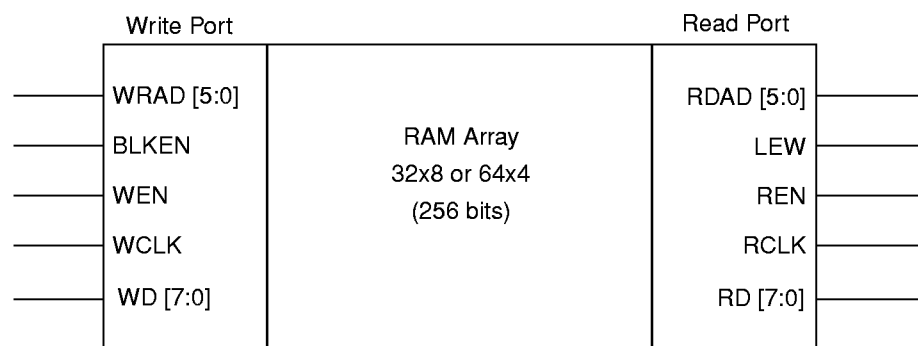
Output Buffer Latches (ACT 2 and 1200XL/3200DX)



Decode Module Timing

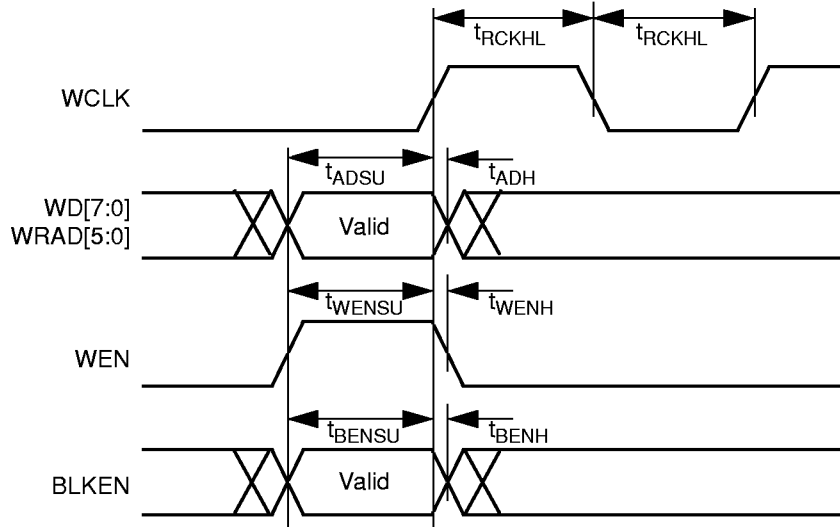


SRAM Timing Characteristics



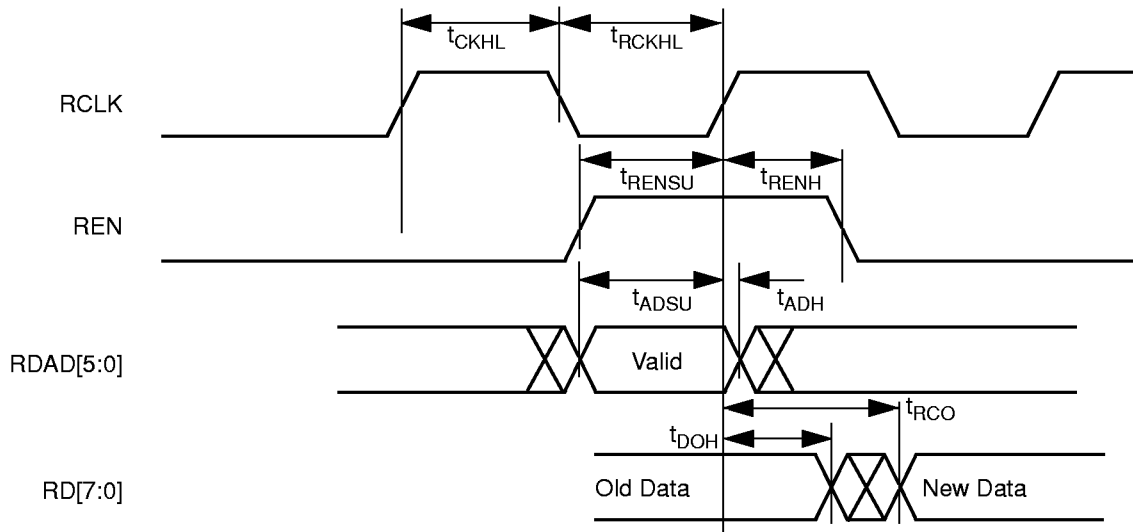
Dual-Port SRAM Timing Waveforms

3200DX SRAM Write Operation



Note: Identical timing for falling-edge clock.

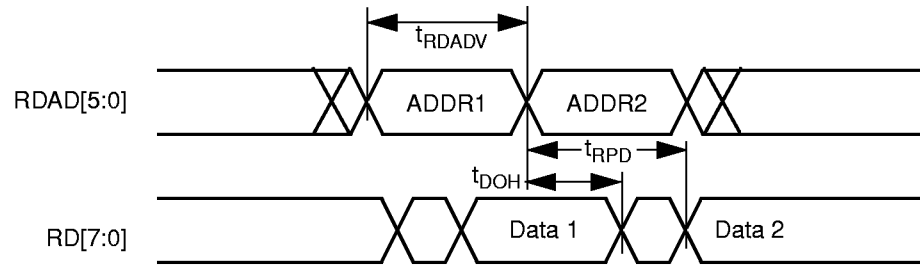
3200DX SRAM Synchronous Read Operation



Note: Identical timing for falling-edge clock.

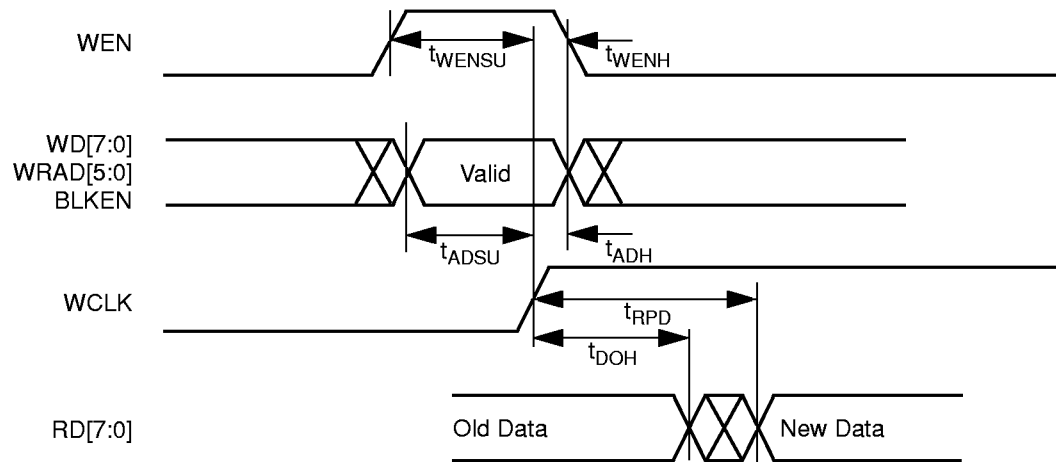
3200DX SRAM Asynchronous Read Operation—Type 1

(Read Address Controlled)



3200DX SRAM Asynchronous Read Operation—Type 2

(Write Address Controlled)



ACT 1 Timing Characteristics

(Worst-Case Military Conditions)

| Logic Module Propagation Delays | | -1 Speed | | Std Speed | | |
|--|--|----------|------|-----------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| t _{PD1} | Single Module | | 4.7 | | 5.5 | ns |
| t _{PD2} | Dual Module Macros | | 10.8 | | 12.7 | ns |
| t _{CO} | Sequential Clk to Q | | 4.7 | | 5.5 | ns |
| t _{GO} | Latch G to Q | | 4.7 | | 5.5 | ns |
| t _{RS} | Flip-Flop (Latch) Reset to Q | | 4.7 | | 5.5 | ns |
| Predicted Routing Delays¹ | | | | | | |
| t _{RD1} | FO=1 Routing Delay | | 1.5 | | 1.7 | ns |
| t _{RD2} | FO=2 Routing Delay | | 2.3 | | 2.7 | ns |
| t _{RD3} | FO=3 Routing Delay | | 3.4 | | 4.0 | ns |
| t _{RD4} | FO=4 Routing Delay | | 5.0 | | 5.9 | ns |
| t _{RD8} | FO=8 Routing Delay | | 10.6 | | 12.5 | ns |
| Sequential Timing Characteristics² | | | | | | |
| t _{SUD} | Flip-Flop (Latch) Data Input Setup | 8.8 | | 10.4 | | ns |
| t _{HD} | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | ns |
| t _{SUENA} | Flip-Flop (Latch) Enable Setup | 8.8 | | 10.4 | | ns |
| t _{HENA} | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | ns |
| t _{WCLKA} | Flip-Flop (Latch) Clock Active Pulse Width | 10.9 | | 12.9 | | ns |
| t _{WASYN} | Flip-Flop (Latch) Asynchronous Pulse Width | 10.9 | | 12.9 | | ns |
| t _A | Flip-Flop Clock Input Period | 23.2 | | 27.3 | | ns |
| f _{MAX} | Flip-Flop (Latch) Clock Frequency | | 44 | | 37 | MHz |

Notes:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
2. Setup times assume fanout of 3. Further derating information can be obtained from the DirectTime Analyzer utility.

ACT 1 Timing Characteristics (continued)

(Worst-Case Military Conditions)

| Input Module Propagation Delays | | | -1 Speed | | Std Speed | | |
|--|--------------------------|----------|----------|------|-----------|------|-------|
| Parameter | Description | | Min. | Max. | Min. | Max. | Units |
| t _{INYH} | Pad to Y High | | | 4.9 | | 5.8 | ns |
| t _{INYL} | Pad to Y Low | | | 4.9 | | 5.8 | ns |
| Input Module Predicted Routing Delays ¹ | | | | | | | |
| t _{IRD1} | FO=1 Routing Delay | | | 1.5 | | 1.7 | ns |
| t _{IRD2} | FO=2 Routing Delay | | | 2.3 | | 2.7 | ns |
| t _{IRD3} | FO=3 Routing Delay | | | 3.4 | | 4.0 | ns |
| t _{IRD4} | FO=4 Routing Delay | | | 5.0 | | 5.9 | ns |
| t _{IRD8} | FO=8 Routing Delay | | | 10.6 | | 12.5 | ns |
| Global Clock Network | | | | | | | |
| t _{CKH} | Input Low to High | FO = 16 | | 7.8 | | 9.2 | ns |
| | | FO = 128 | | 8.9 | | 10.5 | |
| t _{CKL} | Input High to Low | FO = 16 | | 10.3 | | 12.1 | ns |
| | | FO = 128 | | 11.2 | | 13.2 | |
| t _{PWH} | Minimum Pulse Width High | FO = 16 | 10.4 | | 12.2 | | ns |
| | | FO = 128 | 10.9 | | 12.9 | | |
| t _{PWL} | Minimum Pulse Width Low | FO = 16 | 10.4 | | 12.2 | | ns |
| | | FO = 128 | 10.9 | | 12.9 | | |
| t _{CKSW} | Maximum Skew | FO = 16 | | 1.9 | | 2.2 | ns |
| | | FO = 128 | | 2.9 | | 3.4 | |
| t _P | Minimum Period | FO = 16 | 21.7 | | 25.6 | | ns |
| | | FO = 128 | 23.2 | | 27.3 | | |
| f _{MAX} | Maximum Frequency | FO = 16 | | 46 | | 40 | MHz |
| | | FO = 128 | | 44 | | 37 | |

Note:

1. These parameters should be used for estimating device performance. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

ACT 1 Timing Characteristics (continued)

(Worst-Case Military Conditions)

| Output Module Timing | | -1 Speed | | Std Speed | | |
|--|----------------------|----------|------|-----------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| TTL Output Module Timing¹ | | | | | | |
| t _{DLH} | Data to Pad High | | 12.1 | | 14.2 | ns |
| t _{DHL} | Data to Pad Low | | 13.8 | | 16.3 | ns |
| t _{ENZH} | Enable Pad Z to High | | 12.0 | | 14.1 | ns |
| t _{ENZL} | Enable Pad Z to Low | | 14.6 | | 17.1 | ns |
| t _{ENHZ} | Enable Pad High to Z | | 16.0 | | 18.8 | ns |
| t _{ENLZ} | Enable Pad Low to Z | | 14.5 | | 17.0 | ns |
| d _{TLH} | Delta Low to High | | 0.09 | | 0.11 | ns/pF |
| d _{THL} | Delta High to Low | | 0.12 | | 0.15 | ns/pF |
| CMOS Output Module Timing¹ | | | | | | |
| t _{DLH} | Data to Pad High | | 15.1 | | 17.7 | ns |
| t _{DHL} | Data to Pad Low | | 11.5 | | 13.6 | ns |
| t _{ENZH} | Enable Pad Z to High | | 12.0 | | 14.1 | ns |
| t _{ENZL} | Enable Pad Z to Low | | 14.6 | | 17.1 | ns |
| t _{ENHZ} | Enable Pad High to Z | | 16.0 | | 18.8 | ns |
| t _{ENLZ} | Enable Pad Low to Z | | 14.5 | | 17.0 | ns |
| d _{TLH} | Delta Low to High | | 0.16 | | 0.18 | ns/pF |
| d _{THL} | Delta High to Low | | 0.09 | | 0.11 | ns/pF |

Notes:

1. Delays based on 50 pF loading.
2. SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note.

A1240A Timing Characteristics

(Worst-Case Military Conditions)

| Logic Module Propagation Delays ¹ | | –1 Speed | | Std Speed | | |
|---|--|----------|------|-----------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| t _{PD1} | Single Module | | 5.2 | | 6.1 | ns |
| t _{CO} | Sequential Clk to Q | | 5.2 | | 6.1 | ns |
| t _{GO} | Latch G to Q | | 5.2 | | 6.1 | ns |
| t _{RS} | Flip-Flop (Latch) Reset to Q | | 5.2 | | 6.1 | ns |
| Predicted Routing Delays ² | | | | | | |
| t _{RD1} | FO=1 Routing Delay | | 1.9 | | 2.2 | ns |
| t _{RD2} | FO=2 Routing Delay | | 2.4 | | 2.8 | ns |
| t _{RD3} | FO=3 Routing Delay | | 3.1 | | 3.7 | ns |
| t _{RD4} | FO=4 Routing Delay | | 4.3 | | 5.0 | ns |
| t _{RD8} | FO=8 Routing Delay | | 6.6 | | 7.7 | ns |
| Sequential Timing Characteristics ^{3, 4} | | | | | | |
| t _{SUD} | Flip-Flop (Latch) Data Input Setup | 0.5 | | 0.5 | | ns |
| t _{HD} | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | ns |
| t _{SUENA} | Flip-Flop (Latch) Enable Setup | 1.3 | | 1.3 | | ns |
| t _{HENA} | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | ns |
| t _{WCLKA} | Flip-Flop (Latch) Clock Active Pulse Width | 7.4 | | 8.1 | | ns |
| t _{WASYN} | Flip-Flop (Latch) Asynchronous Pulse Width | 7.4 | | 8.1 | | ns |
| t _A | Flip-Flop Clock Input Period | 14.8 | | 18.6 | | ns |
| t _{INH} | Input Buffer Latch Hold | 2.5 | | 2.5 | | ns |
| t _{INSU} | Input Buffer Latch Setup | –3.5 | | –3.5 | | ns |
| t _{OUTH} | Output Buffer Latch Hold | 0.0 | | 0.0 | | ns |
| t _{OUTSU} | Output Buffer Latch Setup | 0.5 | | 0.5 | | ns |
| f _{MAX} | Flip-Flop (Latch) Clock Frequency | | 63 | | 54 | MHz |

Notes:

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
4. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1240A Timing Characteristics (continued)

(Worst-Case Military Conditions)

| Input Module Propagation Delays | | | -1 Speed | | Std Speed | | |
|--|----------------------------|---------------------|--------------|--------------|--------------|--------------|-------|
| Parameter | Description | | Min. | Max. | Min. | Max. | Units |
| t _{INYH} | Pad to Y High | | | 4.0 | | 4.7 | ns |
| t _{INYL} | Pad to Y Low | | | 3.6 | | 4.3 | ns |
| t _{INGH} | G to Y High | | | 6.9 | | 8.1 | ns |
| t _{INGL} | G to Y Low | | | 6.6 | | 7.7 | ns |
| Input Module Predicted Routing Delays ¹ | | | | | | | |
| t _{IRD1} | FO=1 Routing Delay | | | 5.8 | | 6.9 | ns |
| t _{IRD2} | FO=2 Routing Delay | | | 6.7 | | 7.8 | ns |
| t _{IRD3} | FO=3 Routing Delay | | | 7.5 | | 8.8 | ns |
| t _{IRD4} | FO=4 Routing Delay | | | 8.2 | | 9.7 | ns |
| t _{IRD8} | FO=8 Routing Delay | | | 10.9 | | 12.9 | ns |
| Global Clock Network | | | | | | | |
| t _{CKH} | Input Low to High | FO = 32 FO = 256 | | 13.3 16.3 | | 15.7 19.2 | ns |
| t _{CKL} | Input High to Low | FO = 32 FO = 256 | | 13.3 16.5 | | 15.7 19.5 | ns |
| t _{PWH} | Minimum Pulse Width High | FO = 32 FO = 256 | 5.7 6.0 | | 6.7 7.1 | | ns |
| t _{PWL} | Minimum Pulse Width Low | FO = 32 FO = 256 | 5.7 6.0 | | 6.7 7.1 | | ns |
| t _{CKSW} | Maximum Skew | FO = 32 FO = 256 | | 0.6 3.1 | | 0.6 3.1 | ns |
| t _{SUEXT} | Input Latch External Setup | FO = 32 FO = 256 | 0.0 0.0 | | 0.0 0.0 | | ns |
| t _{HEXT} | Input Latch External Hold | FO = 32 FO = 256 | 8.6 13.8 | | 8.6 13.8 | | ns |
| t _P | Minimum Period | FO = 32 FO = 256 | 11.5 12.2 | | 13.5 14.3 | | ns |
| f _{MAX} | Maximum Frequency | FO = 32 FO = 256 | | 87 82 | | 74 70 | MHz |

Note:

1. These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1240A Timing Characteristics (continued)

(Worst-Case Military Conditions)

| Output Module Timing | | -1 Speed | | Std Speed | | |
|--|----------------------|----------|------|-----------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| TTL Output Module Timing¹ | | | | | | |
| t _{DLH} | Data to Pad High | | 11.0 | | 13.0 | ns |
| t _{DHL} | Data to Pad Low | | 13.9 | | 16.4 | ns |
| t _{ENZH} | Enable Pad Z to High | | 12.3 | | 14.4 | ns |
| t _{ENZL} | Enable Pad Z to Low | | 16.1 | | 19.0 | ns |
| t _{ENHZ} | Enable Pad High to Z | | 9.8 | | 11.5 | ns |
| t _{ENLZ} | Enable Pad Low to Z | | 11.5 | | 13.6 | ns |
| t _{GLH} | G to Pad High | | 12.4 | | 14.6 | ns |
| t _{GHL} | G to Pad Low | | 15.5 | | 18.2 | ns |
| d _{TLH} | Delta Low to High | | 0.09 | | 0.11 | ns/pF |
| d _{THL} | Delta High to Low | | 0.17 | | 0.20 | ns/pF |
| CMOS Output Module Timing¹ | | | | | | |
| t _{DLH} | Data to Pad High | | 14.0 | | 16.5 | ns |
| t _{DHL} | Data to Pad Low | | 11.7 | | 13.7 | ns |
| t _{ENZH} | Enable Pad Z to High | | 12.3 | | 14.4 | ns |
| t _{ENZL} | Enable Pad Z to Low | | 16.1 | | 19.0 | ns |
| t _{ENHZ} | Enable Pad High to Z | | 9.8 | | 11.5 | ns |
| t _{ENLZ} | Enable Pad Low to Z | | 11.5 | | 13.6 | ns |
| t _{GLH} | G to Pad High | | 12.4 | | 14.6 | ns |
| t _{GHL} | G to Pad Low | | 15.5 | | 18.2 | ns |
| d _{TLH} | Delta Low to High | | 0.17 | | 0.20 | ns/pF |
| d _{THL} | Delta High to Low | | 0.12 | | 0.15 | ns/pF |

Notes:

1. Delays based on 50 pF loading.
2. SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note.

A1280A Timing Characteristics

(Worst-Case Military Conditions)

| Logic Module Propagation Delays ¹ | | -1 Speed | | Std Speed | | |
|---|--|----------|------|-----------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| t _{PD1} | Single Module | | 5.2 | | 6.1 | ns |
| t _{CO} | Sequential Clk to Q | | 5.2 | | 6.1 | ns |
| t _{GO} | Latch G to Q | | 5.2 | | 6.1 | ns |
| t _{RS} | Flip-Flop (Latch) Reset to Q | | 5.2 | | 6.1 | ns |
| Predicted Routing Delays ² | | | | | | |
| t _{RD1} | FO=1 Routing Delay | | 2.4 | | 2.8 | ns |
| t _{RD2} | FO=2 Routing Delay | | 3.4 | | 4.0 | ns |
| t _{RD3} | FO=3 Routing Delay | | 4.2 | | 4.9 | ns |
| t _{RD4} | FO=4 Routing Delay | | 5.1 | | 6.0 | ns |
| t _{RD8} | FO=8 Routing Delay | | 9.2 | | 10.8 | ns |
| Sequential Timing Characteristics ^{3, 4} | | | | | | |
| t _{SUD} | Flip-Flop (Latch) Data Input Setup | 0.5 | | 0.5 | | ns |
| t _{HD} | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | ns |
| t _{SUENA} | Flip-Flop (Latch) Enable Setup | 1.3 | | 1.3 | | ns |
| t _{HENA} | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | ns |
| t _{WCLKA} | Flip-Flop (Latch) Clock Active Pulse Width | 7.4 | | 8.6 | | ns |
| t _{WASYN} | Flip-Flop (Latch) Asynchronous Pulse Width | 7.4 | | 8.6 | | ns |
| t _A | Flip-Flop Clock Input Period | 16.4 | | 22.1 | | ns |
| t _{INH} | Input Buffer Latch Hold | 2.5 | | 2.5 | | ns |
| t _{INSU} | Input Buffer Latch Setup | -3.5 | | -3.5 | | ns |
| t _{OUTH} | Output Buffer Latch Hold | 0.0 | | 0.0 | | ns |
| t _{OUTSU} | Output Buffer Latch Setup | 0.5 | | 0.5 | | ns |
| f _{MAX} | Flip-Flop (Latch) Clock Frequency | | 60 | | 41 | MHz |

Notes:

- For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
- Setup and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1280A Timing Characteristics (continued)

(Worst-Case Military Conditions)

| Input Module Propagation Delays | | | -1 Speed | | Std Speed | | |
|--|----------------------------|----------|----------|------|-----------|------|-------|
| Parameter | Description | | Min. | Max. | Min. | Max. | Units |
| t _{INYH} | Pad to Y High | | | 4.0 | | 4.7 | ns |
| t _{INYL} | Pad to Y Low | | | 3.6 | | 4.3 | ns |
| t _{INGH} | G to Y High | | | 6.9 | | 8.1 | ns |
| t _{INGL} | G to Y Low | | | 6.6 | | 7.7 | ns |
| Input Module Predicted Routing Delays ¹ | | | | | | | |
| t _{RD1} | FO=1 Routing Delay | | | 6.2 | | 7.3 | ns |
| t _{RD2} | FO=2 Routing Delay | | | 7.2 | | 8.4 | ns |
| t _{RD3} | FO=3 Routing Delay | | | 7.7 | | 9.1 | ns |
| t _{RD4} | FO=4 Routing Delay | | | 8.9 | | 10.5 | ns |
| t _{RD8} | FO=8 Routing Delay | | | 12.9 | | 15.2 | ns |
| Global Clock Network | | | | | | | |
| t _{CKH} | Input Low to High | FO = 32 | | 13.3 | | 15.7 | ns |
| | | FO = 384 | | 17.9 | | 21.1 | |
| t _{CKL} | Input High to Low | FO = 32 | | 13.3 | | 15.7 | ns |
| | | FO = 384 | | 18.2 | | 21.4 | |
| t _{PWH} | Minimum Pulse Width High | FO = 32 | 6.9 | | 8.1 | | ns |
| | | FO = 384 | 7.9 | | 9.3 | | |
| t _{PWL} | Minimum Pulse Width Low | FO = 32 | 6.9 | | 8.1 | | ns |
| | | FO = 384 | 7.9 | | 9.3 | | |
| t _{CKSW} | Maximum Skew | FO = 32 | | 0.6 | | 0.6 | ns |
| | | FO = 384 | | 3.1 | | 3.1 | |
| t _{SUEXT} | Input Latch External Setup | FO = 32 | 0.0 | | 0.0 | | ns |
| | | FO = 384 | 0.0 | | 0.0 | | |
| t _{HEXT} | Input Latch External Hold | FO = 32 | 8.6 | | 8.6 | | ns |
| | | FO = 384 | 13.8 | | 13.8 | | |
| t _P | Minimum Period | FO = 32 | 13.7 | | 16.2 | | ns |
| | | FO = 384 | 16.0 | | 18.9 | | |
| f _{MAX} | Maximum Frequency | FO = 32 | | 73 | | 62 | MHz |
| | | FO = 384 | | 63 | | 53 | |

Note:

1. These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1280A Timing Characteristics (continued)

(Worst-Case Military Conditions)

| Output Module Timing | | -1 Speed | | Std Speed | | |
|--|----------------------|----------|------|-----------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| TTL Output Module Timing¹ | | | | | | |
| t _{DLH} | Data to Pad High | | 11.0 | | 13.0 | ns |
| t _{DHL} | Data to Pad Low | | 13.9 | | 16.4 | ns |
| t _{ENZH} | Enable Pad Z to High | | 12.3 | | 14.4 | ns |
| t _{ENZL} | Enable Pad Z to Low | | 16.1 | | 19.0 | ns |
| t _{ENHZ} | Enable Pad High to Z | | 9.8 | | 11.5 | ns |
| t _{ENLZ} | Enable Pad Low to Z | | 11.5 | | 13.6 | ns |
| t _{GLH} | G to Pad High | | 12.4 | | 14.6 | ns |
| t _{GHL} | G to Pad Low | | 15.5 | | 18.2 | ns |
| d _{TLH} | Delta Low to High | | 0.09 | | 0.11 | ns/pF |
| d _{THL} | Delta High to Low | | 0.17 | | 0.20 | ns/pF |
| CMOS Output Module Timing¹ | | | | | | |
| t _{DLH} | Data to Pad High | | 14.0 | | 16.5 | ns |
| t _{DHL} | Data to Pad Low | | 11.7 | | 13.7 | ns |
| t _{ENZH} | Enable Pad Z to High | | 12.3 | | 14.4 | ns |
| t _{ENZL} | Enable Pad Z to Low | | 16.1 | | 19.0 | ns |
| t _{ENHZ} | Enable Pad High to Z | | 9.8 | | 11.5 | ns |
| t _{ENLZ} | Enable Pad Low to Z | | 11.5 | | 13.6 | ns |
| t _{GLH} | G to Pad High | | 12.4 | | 14.6 | ns |
| t _{GHL} | G to Pad Low | | 15.5 | | 18.2 | ns |
| d _{TLH} | Delta Low to High | | 0.17 | | 0.20 | ns/pF |
| d _{THL} | Delta High to Low | | 0.12 | | 0.15 | ns/pF |

Notes:

1. Delays based on 50 pF loading.
2. SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note.

A1280XL Timing Characteristics

(Worst-Case Military Conditions)

| Logic Module Propagation Delays ¹ | | -1 Speed | | Std Speed | | |
|---|--|----------|------|-----------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| t _{PD1} | Single Module | | 3.7 | | 4.3 | ns |
| t _{CO} | Sequential Clk to Q | | 3.7 | | 4.3 | ns |
| t _{GO} | Latch G to Q | | 3.7 | | 4.3 | ns |
| t _{RS} | Flip-Flop (Latch) Reset to Q | | 3.7 | | 4.3 | ns |
| Predicted Routing Delays ² | | | | | | |
| t _{RD1} | FO=1 Routing Delay | | 1.7 | | 2.1 | ns |
| t _{RD2} | FO=2 Routing Delay | | 2.5 | | 3.0 | ns |
| t _{RD3} | FO=3 Routing Delay | | 3.1 | | 3.6 | ns |
| t _{RD4} | FO=4 Routing Delay | | 3.7 | | 4.3 | ns |
| t _{RD8} | FO=8 Routing Delay | | 7.0 | | 8.3 | ns |
| Sequential Timing Characteristics ^{3, 4} | | | | | | |
| t _{SUD} | Flip-Flop (Latch) Data Input Setup | 0.4 | | 0.5 | | ns |
| t _{HD} | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | ns |
| t _{SUENA} | Flip-Flop (Latch) Enable Setup | 1.1 | | 1.2 | | ns |
| t _{HENA} | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | ns |
| t _{WCLKA} | Flip-Flop (Latch) Clock Active Pulse Width | 5.3 | | 6.1 | | ns |
| t _{WASYN} | Flip-Flop (Latch) Asynchronous Pulse Width | 5.3 | | 6.1 | | ns |
| t _A | Flip-Flop Clock Input Period | 10.7 | | 12.3 | | ns |
| t _{INH} | Input Buffer Latch Hold | 0.0 | | 0.0 | | ns |
| t _{INSU} | Input Buffer Latch Setup | 0.4 | | 0.4 | | ns |
| t _{OUTH} | Output Buffer Latch Hold | 0.0 | | 0.0 | | ns |
| t _{OUTSU} | Output Buffer Latch Setup | 0.4 | | 0.4 | | ns |
| f _{MAX} | Flip-Flop (Latch) Clock Frequency | | 90 | | 75 | MHz |

Notes:

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
4. Setup and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1280XL Timing Characteristics (continued)

(Worst-Case Military Conditions)

| Input Module Propagation Delays | | | -1 Speed | | Std Speed | | |
|--|----------------------------|----------|----------|------|-----------|------|-------|
| Parameter | Description | | Min. | Max. | Min. | Max. | Units |
| t _{INYH} | Pad to Y High | | | 1.5 | | 1.7 | ns |
| t _{INYL} | Pad to Y Low | | | 1.7 | | 2.1 | ns |
| t _{INGH} | G to Y High | | | 2.8 | | 3.3 | ns |
| t _{INGL} | G to Y Low | | | 3.7 | | 4.3 | ns |
| Input Module Predicted Routing Delays ¹ | | | | | | | |
| t _{RD1} | FO=1 Routing Delay | | | 4.6 | | 5.3 | ns |
| t _{RD2} | FO=2 Routing Delay | | | 5.2 | | 6.1 | ns |
| t _{RD3} | FO=3 Routing Delay | | | 5.5 | | 6.5 | ns |
| t _{RD4} | FO=4 Routing Delay | | | 6.4 | | 7.5 | ns |
| t _{RD8} | FO=8 Routing Delay | | | 9.2 | | 10.8 | ns |
| Global Clock Network | | | | | | | |
| t _{CKH} | Input Low to High | FO = 32 | | 7.1 | | 8.4 | ns |
| | | FO = 384 | | 8.0 | | 9.5 | |
| t _{CKL} | Input High to Low | FO = 32 | | 7.0 | | 8.3 | ns |
| | | FO = 384 | | 8.0 | | 9.5 | |
| t _{PWH} | Minimum Pulse Width High | FO = 32 | 4.3 | | 5.3 | | ns |
| | | FO = 384 | 4.8 | | 5.7 | | |
| t _{PWL} | Minimum Pulse Width Low | FO = 32 | 4.3 | | 5.3 | | ns |
| | | FO = 384 | 4.8 | | 5.7 | | |
| t _{CKSW} | Maximum Skew | FO = 32 | | 1.1 | | 1.2 | ns |
| | | FO = 384 | | 1.1 | | 1.2 | |
| t _{SUEXT} | Input Latch External Setup | FO = 32 | 0.0 | | 0.0 | | ns |
| | | FO = 384 | 0.0 | | 0.0 | | |
| t _{HEXT} | Input Latch External Hold | FO = 32 | 3.6 | | 4.2 | | ns |
| | | FO = 384 | 4.6 | | 5.3 | | |
| t _P | Minimum Period | FO = 32 | 9.1 | | 10.7 | | ns |
| | | FO = 384 | 9.8 | | 11.8 | | |
| f _{MAX} | Maximum Frequency | FO = 32 | | 110 | | 90 | MHz |
| | | FO = 384 | | 100 | | 85 | |

Note:

1. These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1280XL Timing Characteristics (continued)

(Worst-Case Military Conditions)

| Output Module Timing | | -1 Speed | | Std Speed | | |
|--|----------------------|----------|------|-----------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| TTL Output Module Timing¹ | | | | | | |
| t _{DLH} | Data to Pad High | | 5.3 | | 6.2 | ns |
| t _{DHL} | Data to Pad Low | | 5.7 | | 6.6 | ns |
| t _{ENZH} | Enable Pad Z to High | | 5.3 | | 6.2 | ns |
| t _{ENZL} | Enable Pad Z to Low | | 5.8 | | 6.8 | ns |
| t _{ENHZ} | Enable Pad High to Z | | 7.5 | | 8.9 | ns |
| t _{ENLZ} | Enable Pad Low to Z | | 7.5 | | 8.9 | ns |
| t _{GLH} | G to Pad High | | 5.9 | | 6.9 | ns |
| t _{GHL} | G to Pad Low | | 6.6 | | 7.8 | ns |
| d _{TLH} | Delta Low to High | | 0.05 | | 0.06 | ns/pF |
| d _{THL} | Delta High to Low | | 0.05 | | 0.09 | ns/pF |
| CMOS Output Module Timing¹ | | | | | | |
| t _{DLH} | Data to Pad High | | 6.6 | | 7.9 | ns |
| t _{DHL} | Data to Pad Low | | 4.7 | | 5.5 | ns |
| t _{ENZH} | Enable Pad Z to High | | 5.3 | | 6.2 | ns |
| t _{ENZL} | Enable Pad Z to Low | | 5.8 | | 6.8 | ns |
| t _{ENHZ} | Enable Pad High to Z | | 7.5 | | 8.9 | ns |
| t _{ENLZ} | Enable Pad Low to Z | | 7.5 | | 8.9 | ns |
| t _{GLH} | G to Pad High | | 5.9 | | 6.9 | ns |
| t _{GHL} | G to Pad Low | | 6.6 | | 7.8 | ns |
| d _{TLH} | Delta Low to High | | 0.07 | | 0.09 | ns/pF |
| d _{THL} | Delta High to Low | | 0.06 | | 0.09 | ns/pF |

Notes:

1. Delays based on 50 pF loading.
2. SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note.

A1425A Timing Characteristics

(Worst-Case Military Conditions)

| Logic Module Propagation Delays ¹ | | -1 Speed | | Std Speed | | |
|--|------------------------------------|----------|------|-----------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| t _{PD} | Internal Array Module | | 3.0 | | 3.5 | ns |
| t _{CO} | Sequential Clock to Q | | 3.0 | | 3.5 | ns |
| t _{CLR} | Asynchronous Clear to Q | | 3.0 | | 3.5 | ns |
| Predicted Routing Delays ² | | | | | | |
| t _{RD1} | FO=1 Routing Delay | | 1.3 | | 1.5 | ns |
| t _{RD2} | FO=2 Routing Delay | | 1.9 | | 2.1 | ns |
| t _{RD3} | FO=3 Routing Delay | | 2.1 | | 2.5 | ns |
| t _{RD4} | FO=4 Routing Delay | | 2.6 | | 2.9 | ns |
| t _{RD8} | FO=8 Routing Delay | | 4.2 | | 4.9 | ns |
| Logic Module Sequential Timing | | | | | | |
| t _{SUD} | Flip-Flop (Latch) Data Input Setup | 0.9 | | 1.0 | | ns |
| t _{HD} | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | ns |
| t _{SUENA} | Flip-Flop (Latch) Enable Setup | 0.9 | | 1.0 | | ns |
| t _{HENA} | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | ns |
| t _{WASYN} | Asynchronous Pulse Width | 3.8 | | 4.4 | | ns |
| t _{WCLKA} | Flip-Flop Clock Pulse Width | 3.8 | | 4.4 | | ns |
| t _A | Flip-Flop Clock Input Period | 7.9 | | 9.3 | | ns |
| f _{MAX} | Flip-Flop Clock Frequency | | 125 | | 100 | MHz |

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1425A Timing Characteristics (continued)

(Worst-Case Military Conditions)

| I/O Module Input Propagation Delays | | -1 Speed | | Std Speed | | |
|---|--|----------|------|-----------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| t _{INY} | Input Data Pad to Y | | 4.2 | | 4.9 | ns |
| t _{ICKY} | Input Reg IOCLK Pad to Y | | 7.0 | | 8.2 | ns |
| t _{OCKY} | Output Reg IOCLK Pad to Y | | 7.0 | | 8.2 | ns |
| t _{ICLRY} | Input Asynchronous Clear to Y | | 7.0 | | 8.2 | ns |
| t _{OCLRY} | Output Asynchronous Clear to Y | | 7.0 | | 8.2 | ns |
| Predicted Input Routing Delays¹ | | | | | | |
| t _{IRD1} | FO=1 Routing Delay | | 1.3 | | 1.5 | ns |
| t _{IRD2} | FO=2 Routing Delay | | 1.9 | | 2.1 | ns |
| t _{IRD3} | FO=3 Routing Delay | | 2.1 | | 2.5 | ns |
| t _{IRD4} | FO=4 Routing Delay | | 2.6 | | 2.9 | ns |
| t _{IRD8} | FO=8 Routing Delay | | 4.2 | | 4.9 | ns |
| I/O Module Sequential Timing | | | | | | |
| t _{INH} | Input F-F Data Hold (w.r.t. IOCLK Pad) | 0.0 | | 0.0 | | ns |
| t _{INSU} | Input F-F Data Setup (w.r.t. IOCLK Pad) | 2.1 | | 2.4 | | ns |
| t _{IDEH} | Input Data Enable Hold (w.r.t. IOCLK Pad) | 0.0 | | 0.0 | | ns |
| t _{IDESU} | Input Data Enable Setup (w.r.t. IOCLK Pad) | 8.7 | | 10.0 | | ns |
| t _{OUTH} | Output F-F Data Hold (w.r.t. IOCLK Pad) | 1.1 | | 1.2 | | ns |
| t _{OUTSU} | Output F-F Data Setup (w.r.t. IOCLK Pad) | 1.1 | | 1.2 | | ns |
| t _{ODEH} | Output Data Enable Hold (w.r.t. IOCLK Pad) | 0.5 | | 0.6 | | ns |
| t _{ODESU} | Output Data Enable Setup (w.r.t. IOCLK Pad) | 2.0 | | 2.4 | | ns |

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1425A Timing Characteristics (continued)

(Worst-Case Military Conditions)

| I/O Module – TTL Output Timing ¹ | | –1 Speed | | Std Speed | | |
|--|----------------------------------|----------|------|-----------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| t _{DHS} | Data to Pad, High Slew | | 7.5 | | 8.9 | ns |
| t _{DLS} | Data to Pad, Low Slew | | 11.9 | | 14.0 | ns |
| t _{ENZHS} | Enable to Pad, Z to H/L, Hi Slew | | 6.0 | | 7.0 | ns |
| t _{ENZLS} | Enable to Pad, Z to H/L, Lo Slew | | 10.9 | | 12.8 | ns |
| t _{ENHSZ} | Enable to Pad, H/L to Z, Hi Slew | | 9.9 | | 11.6 | ns |
| t _{ENLSZ} | Enable to Pad, H/L to Z, Lo Slew | | 9.9 | | 11.6 | ns |
| t _{CKHS} | IOCLK Pad to Pad H/L, Hi Slew | | 10.5 | | 11.6 | ns |
| t _{CKLS} | IOCLK Pad to Pad H/L, Lo Slew | | 15.7 | | 17.4 | ns |
| d _{TLHHS} | Delta Low to High, Hi Slew | | 0.04 | | 0.04 | ns/pF |
| d _{TLHLS} | Delta Low to High, Lo Slew | | 0.07 | | 0.08 | ns/pF |
| d _{THLHS} | Delta High to Low, Hi Slew | | 0.05 | | 0.06 | ns/pF |
| d _{THLLS} | Delta High to Low, Lo Slew | | 0.07 | | 0.08 | ns/pF |
| I/O Module – CMOS Output Timing ¹ | | | | | | |
| t _{DHS} | Data to Pad, High Slew | | 9.2 | | 10.8 | ns |
| t _{DLS} | Data to Pad, Low Slew | | 17.3 | | 20.3 | ns |
| t _{ENZHS} | Enable to Pad, Z to H/L, Hi Slew | | 7.7 | | 9.1 | ns |
| t _{ENZLS} | Enable to Pad, Z to H/L, Lo Slew | | 13.1 | | 15.5 | ns |
| t _{ENHSZ} | Enable to Pad, H/L to Z, Hi Slew | | 9.9 | | 11.6 | ns |
| t _{ENLSZ} | Enable to Pad, H/L to Z, Lo Slew | | 10.5 | | 11.6 | ns |
| t _{CKHS} | IOCLK Pad to Pad H/L, Hi Slew | | 12.5 | | 13.7 | ns |
| t _{CKLS} | IOCLK Pad to Pad H/L, Lo Slew | | 18.1 | | 20.1 | ns |
| d _{TLHHS} | Delta Low to High, Hi Slew | | 0.06 | | 0.07 | ns/pF |
| d _{TLHLS} | Delta Low to High, Lo Slew | | 0.11 | | 0.13 | ns/pF |
| d _{THLHS} | Delta High to Low, Hi Slew | | 0.04 | | 0.05 | ns/pF |
| d _{THLLS} | Delta High to Low, Lo Slew | | 0.05 | | 0.06 | ns/pF |

Notes:

1. Delays based on 35 pF loading.
2. SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note.

A1425A Timing Characteristics (continued)

(Worst-Case Military Conditions)

| Dedicated (Hard-Wired) I/O Clock Network | | -1 Speed | | Std Speed | | |
|---|--|-----------------|-------------|------------------|-------------|--------------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| t_{IOCKH} | Input Low to High (Pad to I/O Module Input) | | 3.0 | | 3.5 | ns |
| t_{IOPWH} | Minimum Pulse Width High | 3.9 | | 4.4 | | ns |
| t_{IOPWL} | Minimum Pulse Width Low | 3.9 | | 4.4 | | ns |
| t_{IOSAPW} | Minimum Asynchronous Pulse Width | 3.9 | | 4.4 | | ns |
| t_{IOCKSW} | Maximum Skew | | 0.5 | | 0.5 | ns |
| t_{IOP} | Minimum Period | 7.9 | | 9.3 | | ns |
| f_{IOMAX} | Maximum Frequency | | 125 | | 100 | MHz |
| Dedicated (Hard-Wired) Array Clock Network | | | | | | |
| t_{HCKH} | Input Low to High (Pad to S-Module Input) | | 4.6 | | 5.3 | ns |
| t_{HCKL} | Input High to Low (Pad to S-Module Input) | | 4.6 | | 5.3 | ns |
| t_{HPWH} | Minimum Pulse Width High | 3.9 | | 4.4 | | ns |
| t_{HPWL} | Minimum Pulse Width Low | 3.9 | | 4.4 | | ns |
| t_{HCKSW} | Maximum Skew | | 0.4 | | 0.4 | ns |
| t_{HP} | Minimum Period | 7.9 | | 9.3 | | ns |
| f_{HMAX} | Maximum Frequency | | 125 | | 100 | MHz |
| Routed Array Clock Networks | | | | | | |
| t_{RCKH} | Input Low to High (FO=64) | | 5.5 | | 6.4 | ns |
| t_{RCKL} | Input High to Low (FO=64) | | 6.0 | | 7.0 | ns |
| t_{RPWH} | Min. Pulse Width High (FO=64) | 4.9 | | 5.7 | | ns |
| t_{RPWL} | Min. Pulse Width Low (FO=64) | 4.9 | | 5.7 | | ns |
| t_{RCKSW} | Maximum Skew (FO=128) | | 1.1 | | 1.2 | ns |
| t_{RP} | Minimum Period (FO=64) | 10.1 | | 11.6 | | ns |
| f_{RMAX} | Maximum Frequency (FO=64) | | 100 | | 85 | MHz |
| Clock-to-Clock Skews | | | | | | |
| $t_{IOHCKSW}$ | I/O Clock to H-Clock Skew | 0.0 | 3.0 | 0.0 | 3.0 | ns |
| $t_{IORCKSW}$ | I/O Clock to R-Clock Skew | 0.0 | 3.0 | 0.0 | 3.0 | ns |
| t_{HRCKSW} | H-Clock to R-Clock Skew (FO = 64) | 0.0 | 1.0 | 0.0 | 1.0 | ns |
| | (FO = 50% max.) | 0.0 | 3.0 | 0.0 | 3.0 | ns |

Note:

1. Delays based on 35 pF loading.

A1460A Timing Characteristics

(Worst-Case Military Conditions)

| Logic Module Propagation Delays ¹ | | -1 Speed | | Std Speed | | |
|--|------------------------------------|----------|------|-----------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| t _{PD} | Internal Array Module | | 3.0 | | 3.5 | ns |
| t _{CO} | Sequential Clock to Q | | 3.0 | | 3.5 | ns |
| t _{CLR} | Asynchronous Clear to Q | | 3.0 | | 3.5 | ns |
| Predicted Routing Delays ² | | | | | | |
| t _{RD1} | FO=1 Routing Delay | | 1.3 | | 1.5 | ns |
| t _{RD2} | FO=2 Routing Delay | | 1.9 | | 2.1 | ns |
| t _{RD3} | FO=3 Routing Delay | | 2.1 | | 2.5 | ns |
| t _{RD4} | FO=4 Routing Delay | | 2.6 | | 2.9 | ns |
| t _{RD8} | FO=8 Routing Delay | | 4.2 | | 4.9 | ns |
| Logic Module Sequential Timing | | | | | | |
| t _{SUD} | Flip-Flop (Latch) Data Input Setup | 0.9 | | 1.0 | | ns |
| t _{HD} | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | ns |
| t _{SUENA} | Flip-Flop (Latch) Enable Setup | 0.9 | | 1.0 | | ns |
| t _{HENA} | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | ns |
| t _{WASYN} | Asynchronous Pulse Width | 4.8 | | 5.6 | | ns |
| t _{WCLKA} | Flip-Flop Clock Pulse Width | 4.8 | | 5.6 | | ns |
| t _A | Flip-Flop Clock Input Period | 9.9 | | 11.6 | | ns |
| f _{MAX} | Flip-Flop Clock Frequency | | 100 | | 85 | MHz |

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1460A Timing Characteristics (continued)

(Worst-Case Military Conditions)

| I/O Module Input Propagation Delays | | -1 Speed | | Std Speed | | |
|---|--|----------|------|-----------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| $t_{IN Y}$ | Input Data Pad to Y | | 4.2 | | 4.9 | ns |
| $t_{ICK Y}$ | Input Reg IOCLK Pad to Y | | 7.0 | | 8.2 | ns |
| $t_{OCK Y}$ | Output Reg IOCLK Pad to Y | | 7.0 | | 8.2 | ns |
| $t_{ICLR Y}$ | Input Asynchronous Clear to Y | | 7.0 | | 8.2 | ns |
| $t_{OCLR Y}$ | Output Asynchronous Clear to Y | | 7.0 | | 8.2 | ns |
| Predicted Input Routing Delays¹ | | | | | | |
| t_{IRD1} | FO=1 Routing Delay | | 1.3 | | 1.5 | ns |
| t_{IRD2} | FO=2 Routing Delay | | 1.9 | | 2.1 | ns |
| t_{IRD3} | FO=3 Routing Delay | | 2.1 | | 2.5 | ns |
| t_{IRD4} | FO=4 Routing Delay | | 2.6 | | 2.9 | ns |
| t_{IRD8} | FO=8 Routing Delay | | 4.2 | | 4.9 | ns |
| I/O Module Sequential Timing | | | | | | |
| t_{INH} | Input F-F Data Hold (w.r.t. IOCLK Pad) | 0.0 | | 0.0 | | ns |
| t_{INSU} | Input F-F Data Setup (w.r.t. IOCLK Pad) | 2.1 | | 2.4 | | ns |
| t_{IDEH} | Input Data Enable Hold (w.r.t. IOCLK Pad) | 0.0 | | 0.0 | | ns |
| t_{IDESU} | Input Data Enable Setup (w.r.t. IOCLK Pad) | 8.7 | | 10.0 | | ns |
| t_{OUTH} | Output F-F Data Hold (w.r.t. IOCLK Pad) | 1.1 | | 1.2 | | ns |
| t_{OUTSU} | Output F-F Data Setup (w.r.t. IOCLK Pad) | 1.1 | | 1.2 | | ns |
| t_{ODEH} | Output Data Enable Hold (w.r.t. IOCLK Pad) | 0.5 | | 0.6 | | ns |
| t_{ODESU} | Output Data Enable Setup (w.r.t. IOCLK Pad) | 2.0 | | 2.4 | | ns |

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1460A Timing Characteristics (continued)

(Worst-Case Military Conditions)

| I/O Module – TTL Output Timing ¹ | | –1 Speed | | Std Speed | | |
|--|----------------------------------|----------|------|-----------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| t _{DHS} | Data to Pad, High Slew | | 7.5 | | 8.9 | ns |
| t _{DLS} | Data to Pad, Low Slew | | 11.9 | | 14.0 | ns |
| t _{ENZHS} | Enable to Pad, Z to H/L, Hi Slew | | 6.0 | | 7.0 | ns |
| t _{ENZLS} | Enable to Pad, Z to H/L, Lo Slew | | 10.9 | | 12.8 | ns |
| t _{ENHSZ} | Enable to Pad, H/L to Z, Hi Slew | | 11.5 | | 13.5 | ns |
| t _{ENLSZ} | Enable to Pad, H/L to Z, Lo Slew | | 10.9 | | 12.8 | ns |
| t _{CKHS} | IOCLK Pad to Pad H/L, Hi Slew | | 11.6 | | 13.4 | ns |
| t _{CKLS} | IOCLK Pad to Pad H/L, Lo Slew | | 17.8 | | 19.8 | ns |
| d _{TLHHS} | Delta Low to High, Hi Slew | | 0.04 | | 0.04 | ns/pF |
| d _{TLHLS} | Delta Low to High, Lo Slew | | 0.07 | | 0.08 | ns/pF |
| d _{THLHS} | Delta High to Low, Hi Slew | | 0.05 | | 0.06 | ns/pF |
| d _{THLLS} | Delta High to Low, Lo Slew | | 0.07 | | 0.08 | ns/pF |
| I/O Module – CMOS Output Timing ¹ | | | | | | |
| t _{DHS} | Data to Pad, High Slew | | 9.2 | | 10.8 | ns |
| t _{DLS} | Data to Pad, Low Slew | | 17.3 | | 20.3 | ns |
| t _{ENZHS} | Enable to Pad, Z to H/L, Hi Slew | | 7.7 | | 9.1 | ns |
| t _{ENZLS} | Enable to Pad, Z to H/L, Lo Slew | | 13.1 | | 15.5 | ns |
| t _{ENHSZ} | Enable to Pad, H/L to Z, Hi Slew | | 10.9 | | 12.8 | ns |
| t _{ENLSZ} | Enable to Pad, H/L to Z, Lo Slew | | 10.9 | | 12.8 | ns |
| t _{CKHS} | IOCLK Pad to Pad H/L, Hi Slew | | 14.1 | | 16.0 | ns |
| t _{CKLS} | IOCLK Pad to Pad H/L, Lo Slew | | 20.2 | | 22.4 | ns |
| d _{TLHHS} | Delta Low to High, Hi Slew | | 0.06 | | 0.07 | ns/pF |
| d _{TLHLS} | Delta Low to High, Lo Slew | | 0.11 | | 0.13 | ns/pF |
| d _{THLHS} | Delta High to Low, Hi Slew | | 0.04 | | 0.05 | ns/pF |
| d _{THLLS} | Delta High to Low, Lo Slew | | 0.05 | | 0.06 | ns/pF |

Notes:

1. Delays based on 35 pF loading.
2. SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note.

A1460A Timing Characteristics (continued)

(Worst-Case Military Conditions)

| Dedicated (Hard-Wired) I/O Clock Network | | -1 Speed | | Std Speed | | |
|---|--|-----------------|-------------|------------------|-------------|--------------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| t_{IOCKH} | Input Low to High (Pad to I/O Module Input) | | 3.5 | | 4.1 | ns |
| t_{IOPWH} | Minimum Pulse Width High | 4.8 | | 5.7 | | ns |
| t_{IOPWL} | Minimum Pulse Width Low | 4.8 | | 5.7 | | ns |
| t_{IOSAPW} | Minimum Asynchronous Pulse Width | 3.9 | | 4.4 | | ns |
| t_{IOCKSW} | Maximum Skew | | 0.9 | | 1.0 | ns |
| t_{IOP} | Minimum Period | 9.9 | | 11.6 | | ns |
| f_{IOMAX} | Maximum Frequency | | 100 | | 85 | MHz |
| Dedicated (Hard-Wired) Array Clock Network | | | | | | |
| t_{HCKH} | Input Low to High (Pad to S-Module Input) | | 5.5 | | 6.4 | ns |
| t_{HCKL} | Input High to Low (Pad to S-Module Input) | | 5.5 | | 6.4 | ns |
| t_{HPWH} | Minimum Pulse Width High | 4.8 | | 5.7 | | ns |
| t_{HPWL} | Minimum Pulse Width Low | 4.8 | | 5.7 | | ns |
| t_{HCKSW} | Maximum Skew | | 0.9 | | 1.0 | ns |
| t_{HP} | Minimum Period | 9.9 | | 11.6 | | ns |
| f_{HMAX} | Maximum Frequency | | 100 | | 85 | MHz |
| Routed Array Clock Networks | | | | | | |
| t_{RCKH} | Input Low to High (FO=256) | | 9.0 | | 10.5 | ns |
| t_{RCKL} | Input High to Low (FO=256) | | 9.0 | | 10.5 | ns |
| t_{RPWH} | Min. Pulse Width High (FO=256) | 6.3 | | 7.1 | | ns |
| t_{RPWL} | Min. Pulse Width Low (FO=256) | 6.3 | | 7.1 | | ns |
| t_{RCKSW} | Maximum Skew (FO=128) | | 1.9 | | 2.1 | ns |
| t_{RP} | Minimum Period (FO=256) | 12.9 | | 14.5 | | ns |
| f_{RMAX} | Maximum Frequency (FO=256) | | 75 | | 65 | MHz |
| Clock-to-Clock Skews | | | | | | |
| $t_{IOHCKSW}$ | I/O Clock to H-Clock Skew | 0.0 | 3.0 | 0.0 | 3.0 | ns |
| $t_{IORCKSW}$ | I/O Clock to R-Clock Skew | 0.0 | 5.0 | 0.0 | 5.0 | ns |
| t_{HRCKSW} | H-Clock to R-Clock Skew (FO = 64) | 0.0 | 1.0 | 0.0 | 1.0 | ns |
| | (FO = 50% max.) | 0.0 | 3.0 | 0.0 | 3.0 | ns |

Note:

1. Delays based on 35 pF loading.

A14100A Timing Characteristics

(Worst-Case Military Conditions)

| Logic Module Propagation Delays ¹ | | -1 Speed | | Std Speed | | |
|--|------------------------------------|----------|------|-----------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| t _{PD} | Internal Array Module | | 3.0 | | 3.5 | ns |
| t _{CO} | Sequential Clock to Q | | 3.0 | | 3.5 | ns |
| t _{CLR} | Asynchronous Clear to Q | | 3.0 | | 3.5 | ns |
| Predicted Routing Delays ² | | | | | | |
| t _{RD1} | FO=1 Routing Delay | | 1.3 | | 1.5 | ns |
| t _{RD2} | FO=2 Routing Delay | | 1.9 | | 2.1 | ns |
| t _{RD3} | FO=3 Routing Delay | | 2.1 | | 2.5 | ns |
| t _{RD4} | FO=4 Routing Delay | | 2.6 | | 2.9 | ns |
| t _{RD8} | FO=8 Routing Delay | | 4.2 | | 4.9 | ns |
| Logic Module Sequential Timing | | | | | | |
| t _{SUD} | Flip-Flop (Latch) Data Input Setup | 1.0 | | 1.0 | | ns |
| t _{HD} | Flip-Flop (Latch) Data Input Hold | 0.6 | | 0.6 | | ns |
| t _{SUENA} | Flip-Flop (Latch) Enable Setup | 1.0 | | 1.0 | | ns |
| t _{HENA} | Flip-Flop (Latch) Enable Hold | 0.6 | | 0.6 | | ns |
| t _{WASYN} | Asynchronous Pulse Width | 4.8 | | 5.6 | | ns |
| t _{WCLKA} | Flip-Flop Clock Pulse Width | 4.8 | | 5.6 | | ns |
| t _A | Flip-Flop Clock Input Period | 9.9 | | 11.6 | | ns |
| f _{MAX} | Flip-Flop Clock Frequency | | 100 | | 85 | MHz |

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A14100A Timing Characteristics (continued)

(Worst-Case Military Conditions)

| I/O Module Input Propagation Delays | | -1 Speed | | Std Speed | | |
|---|--|----------|------|-----------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| $t_{IN Y}$ | Input Data Pad to Y | | 4.2 | | 4.9 | ns |
| $t_{ICK Y}$ | Input Reg IOCLK Pad to Y | | 7.0 | | 8.2 | ns |
| $t_{OCK Y}$ | Output Reg IOCLK Pad to Y | | 7.0 | | 8.2 | ns |
| $t_{ICLR Y}$ | Input Asynchronous Clear to Y | | 7.0 | | 8.2 | ns |
| $t_{OCLR Y}$ | Output Asynchronous Clear to Y | | 7.0 | | 8.2 | ns |
| Predicted Input Routing Delays¹ | | | | | | |
| t_{IRD1} | FO=1 Routing Delay | | 1.3 | | 1.5 | ns |
| t_{IRD2} | FO=2 Routing Delay | | 1.9 | | 2.1 | ns |
| t_{IRD3} | FO=3 Routing Delay | | 2.1 | | 2.5 | ns |
| t_{IRD4} | FO=4 Routing Delay | | 2.6 | | 2.9 | ns |
| t_{IRD8} | FO=8 Routing Delay | | 4.2 | | 4.9 | ns |
| I/O Module Sequential Timing | | | | | | |
| t_{INH} | Input F-F Data Hold (w.r.t. IOCLK Pad) | 0.0 | | 0.0 | | ns |
| t_{INSU} | Input F-F Data Setup (w.r.t. IOCLK Pad) | 2.1 | | 2.4 | | ns |
| t_{IDEH} | Input Data Enable Hold (w.r.t. IOCLK Pad) | 0.0 | | 0.0 | | ns |
| t_{IDESU} | Input Data Enable Setup (w.r.t. IOCLK Pad) | 8.7 | | 10.0 | | ns |
| t_{OUTH} | Output F-F Data Hold (w.r.t. IOCLK Pad) | 1.2 | | 1.2 | | ns |
| t_{OUTSU} | Output F-F Data Setup (w.r.t. IOCLK Pad) | 1.2 | | 1.2 | | ns |
| t_{ODEH} | Output Data Enable Hold (w.r.t. IOCLK Pad) | 0.6 | | 0.6 | | ns |
| t_{ODESU} | Output Data Enable Setup (w.r.t. IOCLK Pad) | 2.4 | | 2.4 | | ns |

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A14100A Timing Characteristics (continued)

(Worst-Case Military Conditions)

| I/O Module – TTL Output Timing ¹ | | –1 Speed | | Std Speed | | |
|--|----------------------------------|----------|------|-----------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| t _{DHS} | Data to Pad, High Slew | | 7.5 | | 8.9 | ns |
| t _{DLS} | Data to Pad, Low Slew | | 11.9 | | 14.0 | ns |
| t _{ENZHS} | Enable to Pad, Z to H/L, Hi Slew | | 6.0 | | 7.0 | ns |
| t _{ENZLS} | Enable to Pad, Z to H/L, Lo Slew | | 10.9 | | 12.8 | ns |
| t _{ENHSZ} | Enable to Pad, H/L to Z, Hi Slew | | 11.9 | | 14.0 | ns |
| t _{ENLSZ} | Enable to Pad, H/L to Z, Lo Slew | | 10.9 | | 12.8 | ns |
| t _{CKHS} | IOCLK Pad to Pad H/L, Hi Slew | | 12.2 | | 14.0 | ns |
| t _{CKLS} | IOCLK Pad to Pad H/L, Lo Slew | | 17.8 | | 17.8 | ns |
| d _{TLHHS} | Delta Low to High, Hi Slew | | 0.04 | | 0.04 | ns/pF |
| d _{TLHLS} | Delta Low to High, Lo Slew | | 0.07 | | 0.08 | ns/pF |
| d _{THLHS} | Delta High to Low, Hi Slew | | 0.05 | | 0.06 | ns/pF |
| d _{THLLS} | Delta High to Low, Lo Slew | | 0.07 | | 0.08 | ns/pF |
| I/O Module – CMOS Output Timing ¹ | | | | | | |
| t _{DHS} | Data to Pad, High Slew | | 9.2 | | 10.8 | ns |
| t _{DLS} | Data to Pad, Low Slew | | 17.3 | | 20.3 | ns |
| t _{ENZHS} | Enable to Pad, Z to H/L, Hi Slew | | 7.7 | | 9.1 | ns |
| t _{ENZLS} | Enable to Pad, Z to H/L, Lo Slew | | 13.1 | | 15.5 | ns |
| t _{ENHSZ} | Enable to Pad, H/L to Z, Hi Slew | | 11.6 | | 14.0 | ns |
| t _{ENLSZ} | Enable to Pad, H/L to Z, Lo Slew | | 10.9 | | 12.8 | ns |
| t _{CKHS} | IOCLK Pad to Pad H/L, Hi Slew | | 14.4 | | 16.0 | ns |
| t _{CKLS} | IOCLK Pad to Pad H/L, Lo Slew | | 20.2 | | 22.4 | ns |
| d _{TLHHS} | Delta Low to High, Hi Slew | | 0.06 | | 0.07 | ns/pF |
| d _{TLHLS} | Delta Low to High, Lo Slew | | 0.11 | | 0.13 | ns/pF |
| d _{THLHS} | Delta High to Low, Hi Slew | | 0.04 | | 0.05 | ns/pF |
| d _{THLLS} | Delta High to Low, Lo Slew | | 0.05 | | 0.06 | ns/pF |

Notes:

1. Delays based on 35 pF loading.
2. SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note.

A14100A Timing Characteristics (continued)

(Worst-Case Military Conditions)

| Dedicated (Hard-Wired) I/O Clock Network | | -1 Speed | | Std Speed | | |
|---|---|-----------------|-------------|------------------|-------------|--------------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| t_{IOCKH} | Input Low to High (Pad to I/O Module Input) | | 3.5 | | 4.1 | ns |
| t_{IOPWH} | Minimum Pulse Width High | 4.8 | | 5.7 | | ns |
| t_{IOPWL} | Minimum Pulse Width Low | 4.8 | | 5.7 | | ns |
| t_{IOSAPW} | Minimum Asynchronous Pulse Width | 3.9 | | 4.4 | | ns |
| t_{IOCKSW} | Maximum Skew | | 0.9 | | 1.0 | ns |
| t_{IOP} | Minimum Period | 9.9 | | 11.6 | | ns |
| f_{IOMAX} | Maximum Frequency | | 100 | | 85 | MHz |
| Dedicated (Hard-Wired) Array Clock Network | | | | | | |
| t_{HCKH} | Input Low to High (Pad to S-Module Input) | | 5.5 | | 6.4 | ns |
| t_{HCKL} | Input High to Low (Pad to S-Module Input) | | 5.5 | | 6.4 | ns |
| t_{HPWH} | Minimum Pulse Width High | 4.8 | | 5.7 | | ns |
| t_{HPWL} | Minimum Pulse Width Low | 4.8 | | 5.7 | | ns |
| t_{HCKSW} | Maximum Skew | | 0.9 | | 1.0 | ns |
| t_{HP} | Minimum Period | 9.9 | | 11.6 | | ns |
| f_{HMAX} | Maximum Frequency | | 100 | | 85 | MHz |
| Routed Array Clock Networks | | | | | | |
| t_{RCKH} | Input Low to High (FO=256) | | 9.0 | | 10.5 | ns |
| t_{RCKL} | Input High to Low (FO=256) | | 9.0 | | 10.5 | ns |
| t_{RPWH} | Min. Pulse Width High (FO=256) | 6.3 | | 7.1 | | ns |
| t_{RPWL} | Min. Pulse Width Low (FO=256) | 6.3 | | 7.1 | | ns |
| t_{RCKSW} | Maximum Skew (FO=128) | | 1.9 | | 2.1 | ns |
| t_{RP} | Minimum Period (FO=256) | 12.9 | | 14.5 | | ns |
| f_{RMAX} | Maximum Frequency (FO=256) | | 75 | | 65 | MHz |
| Clock-to-Clock Skews | | | | | | |
| $t_{IOHCKSW}$ | I/O Clock to H-Clock Skew | 0.0 | 3.5 | 0.0 | 3.5 | ns |
| $t_{IORCKSW}$ | I/O Clock to R-Clock Skew | 0.0 | 5.0 | 0.0 | 5.0 | ns |
| t_{HRCKSW} | H-Clock to R-Clock Skew (FO = 64) (FO = 50% max.) | 0.0 0.0 | 1.0 3.0 | 0.0 0.0 | 1.0 3.0 | ns |

Note:

1. Delays based on 35 pF loading.

A32100DX Timing Characteristics

(Worst-Case Military Conditions)

| Logic Module Propagation Delays | | '-1' Speed | | 'Std' Speed | | |
|--|--|------------|------|-------------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| Combinatorial Functions | | | | | | |
| t _{PD} | Internal Array Module Delay | | 3.1 | | 4.1 | ns |
| t _{PDD} | Internal Decode Module Delay | | 3.3 | | 4.3 | ns |
| Predicted Module Routing Delays | | | | | | |
| t _{RD1} | FO=1 Routing Delay | | 1.3 | | 1.8 | ns |
| t _{RD2} | FO=2 Routing Delay | | 1.9 | | 2.6 | ns |
| t _{RD3} | FO=3 Routing Delay | | 2.6 | | 3.4 | ns |
| t _{RD4} | FO=4 Routing Delay | | 3.3 | | 4.3 | ns |
| t _{RD5} | FO=8 Routing Delay | | 0.6 | | 0.8 | ns |
| t _{RDD} | Decode-to-Output Routing Delay | | 0.5 | | 0.6 | ns |
| Sequential Timing Characteristics | | | | | | |
| t _{CO} | Flip-Flop Clock-to-Output | | 3.1 | | 4.1 | ns |
| t _{GO} | Latch Gate-to-Output | | 3.1 | | 4.1 | ns |
| t _{SU} | Flip-Flop (Latch) Setup Time | 0.5 | | 0.6 | | ns |
| t _H | Flip-Flop (Latch) Hold Time | 0.0 | | 0.0 | | ns |
| t _{RO} | Flip-Flop (Latch) Reset to Output | | 3.1 | | 4.1 | ns |
| t _{SUENA} | Flip-Flop (Latch) Enable Setup | 0.9 | | 1.2 | | ns |
| t _{HENA} | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | ns |
| t _{WCLKA} | Flip-Flop (Latch) Clock Active Pulse Width | 4.3 | | 5.8 | | ns |
| t _{WASYN} | Flip-Flop (Latch) Asynchronous Pulse Width | 5.6 | | 7.5 | | ns |

A32100DX Timing Characteristics (continued)

(Worst-Case Military Conditions)

| Logic Module Timing | | '-1 Speed | | 'Std' Speed | | |
|-------------------------------------|------------------------------------|-----------|------|-------------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| Synchronous SRAM Operations | | | | | | |
| t_{RC} | Read Cycle Time | 8.8 | | 11.8 | | ns |
| t_{WC} | Write Cycle Time | 8.8 | | 11.8 | | ns |
| t_{RCKHL} | Clock High/Low Time | 4.4 | | 5.9 | | ns |
| t_{RCO} | Data Valid After Clock High/Low | | 4.4 | | 5.9 | ns |
| t_{ADSU} | Address/Data Setup Time | 2.1 | | 2.8 | | ns |
| t_{ADH} | Address/Data Hold Time | 0.0 | | 0.0 | | ns |
| t_{RENSU} | Read Enable Setup | 0.8 | | 1.1 | | ns |
| t_{RENH} | Read Enable Hold | 4.4 | | 5.9 | | ns |
| t_{WENSU} | Write Enable Setup | 3.5 | | 4.7 | | ns |
| t_{WENH} | Write Enable Hold | 0.0 | | 0.0 | | ns |
| t_{BENS} | Block Enable Setup | 3.6 | | 4.8 | | ns |
| t_{BENH} | Block Enable Hold | 0.0 | | 0.0 | | ns |
| Asynchronous SRAM Operations | | | | | | |
| t_{RPD} | Asynchronous Access Time | | 10.6 | | 14.1 | ns |
| t_{RDADV} | Read Address Valid | 11.5 | | 15.3 | | ns |
| t_{ADSU} | Address/Data Setup Time | 2.1 | | 2.8 | | ns |
| t_{ADH} | Address/Data Hold Time | 0.0 | | 0.0 | | ns |
| t_{RENSUA} | Read Enable Setup to Address Valid | 0.8 | | 1.1 | | ns |
| t_{RENHA} | Read Enable Hold | 4.4 | | 5.9 | | ns |
| t_{WENSU} | Write Enable Setup | 3.5 | | 4.7 | | ns |
| t_{WENH} | Write Enable Hold | 0.0 | | 0.0 | | ns |
| t_{DOH} | Data Out Hold Time | | 1.6 | | 2.1 | ns |

A32100DX Timing Characteristics (continued)

(Worst-Case Military Conditions)

| Input Module Propagation Delays | | | '-1' Speed | | 'Std' Speed | | |
|---------------------------------------|---|--------|------------|------|-------------|------|-------|
| Parameter | Description | | Min. | Max. | Min. | Max. | Units |
| t _{INPY} | Input Data Pad to Y | | | 1.9 | | 2.6 | ns |
| t _{INGO} | Input Latch Gate-to-Output ¹ | | | 4.0 | | 5.3 | ns |
| t _{INH} | Input Latch Hold ¹ | | 0.0 | | 0.0 | | ns |
| t _{INSU} | Input Latch Setup ¹ | | 0.7 | | 0.9 | | ns |
| t _{ILA} | Latch Active Pulse Width ¹ | | 6.1 | | 8.1 | | ns |
| Input Module Predicted Routing Delays | | | | | | | |
| t _{IRD1} | FO=1 Routing Delay | | | 2.2 | | 2.9 | ns |
| t _{IRD2} | FO=2 Routing Delay | | | 2.8 | | 3.8 | ns |
| t _{IRD3} | FO=3 Routing Delay | | | 3.5 | | 4.7 | ns |
| t _{IRD4} | FO=4 Routing Delay | | | 3.5 | | 4.7 | ns |
| t _{IRD8} | FO=8 Routing Delay | | | 5.6 | | 7.5 | ns |
| Global Clock Network | | | | | | | |
| t _{CKH} | Input Low to High | FO=32 | | 6.5 | | 8.7 | ns |
| | | FO=635 | | 7.9 | | 10.6 | ns |
| t _{CKL} | Input High to Low | FO=32 | | 6.6 | | 8.8 | ns |
| | | FO=635 | | 8.8 | | 11.8 | ns |
| t _{PWH} | Minimum Pulse Width High | FO=32 | 4.1 | | 5.5 | | ns |
| | | FO=635 | 4.6 | | 6.1 | | ns |
| t _{PWL} | Minimum Pulse Width Low | FO=32 | 4.1 | | 5.5 | | ns |
| | | FO=635 | 4.6 | | 6.1 | | ns |
| t _{CKSW} | Maximum Skew | FO=32 | | 1.8 | | 2.4 | ns |
| | | FO=635 | | 1.8 | | 2.4 | ns |
| t _{SUEXT} | Input Latch External Setup | FO=32 | 0.0 | | 0.0 | | ns |
| | | FO=635 | 0.0 | | 0.0 | | ns |
| t _{HEXT} | Input Latch External Hold | FO=32 | 3.0 | | 4.0 | | ns |
| | | FO=635 | 3.8 | | 5.1 | | ns |
| t _P | Minimum Period (1/f _{max}) | FO=32 | 7.1 | | 9.5 | | ns |
| | | FO=635 | 7.9 | | 10.5 | | ns |
| f _{HMAX} | Maximum Datapath Frequency | FO=32 | | 140 | | 105 | MHz |
| | | FO=635 | | 126 | | 95 | MHz |

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.

A32100DX Timing Characteristics (continued)

(Worst-Case Military Conditions)

| Output Module Timing | | '-1' Speed | | 'Std' Speed | | |
|--|---|------------|------|-------------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| TTL Output Module Timing¹ | | | | | | |
| t _{DLH} | Data to Pad High | | 5.1 | | 6.8 | ns |
| t _{DHL} | Data to Pad Low | | 6.3 | | 8.3 | ns |
| t _{ENZH} | Enable Pad Z to High | | 6.6 | | 8.8 | ns |
| t _{ENZL} | Enable Pad Z to Low | | 7.1 | | 9.4 | ns |
| t _{ENHZ} | Enable Pad High to Z | | 11.5 | | 15.3 | ns |
| t _{ENLZ} | Enable Pad Low to Z | | 11.5 | | 15.3 | ns |
| t _{GLH} | G to Pad High | | 11.5 | | 15.3 | ns |
| t _{GHL} | G to Pad Low | | 12.4 | | 16.6 | ns |
| t _{LSU} | I/O Latch Output Setup | 0.4 | | 0.5 | | ns |
| t _{LH} | I/O Latch Output Hold | 0.0 | | 0.0 | | ns |
| t _{LCO} | I/O Latch Clock-Out (Pad-to-Pad) 32 I/O | | 11.5 | | 15.4 | ns |
| t _{ACO} | Array Latch Clock-Out (Pad-to-Pad) 32 I/O | | 16.3 | | 21.7 | ns |
| d _{TLH} | Capacitive Loading, Low to High | | 0.04 | | 0.06 | ns/pF |
| d _{THL} | Capacitive Loading, High to Low | | 0.06 | | 0.08 | ns/pF |
| t _{WDO} | Hard-Wired Wide Decode Output | | 0.05 | | 0.07 | ns |
| CMOS Output Module Timing¹ | | | | | | |
| t _{DLH} | Data to Pad High | | 6.3 | | 8.3 | ns |
| t _{DHL} | Data to Pad Low | | 5.1 | | 6.8 | ns |
| t _{ENZH} | Enable Pad Z to High | | 6.6 | | 8.8 | ns |
| t _{ENZL} | Enable Pad Z to Low | | 7.1 | | 9.4 | ns |
| t _{ENHZ} | Enable Pad High to Z | | 11.5 | | 15.3 | ns |
| t _{ENLZ} | Enable Pad Low to Z | | 11.5 | | 15.3 | ns |
| t _{GLH} | G to Pad High | | 11.5 | | 15.3 | ns |
| t _{GHL} | G to Pad Low | | 12.4 | | 16.6 | ns |
| t _{LSU} | I/O Latch Setup | 0.4 | | 0.5 | | ns |
| t _{LH} | I/O Latch Hold | 0.0 | | 0.0 | | ns |
| t _{LCO} | I/O Latch Clock-Out (Pad-to-Pad) 32 I/O | | 13.7 | | 18.2 | ns |
| t _{ACO} | Array Latch Clock-Out (Pad-to-Pad) 32 I/O | | 19.2 | | 25.6 | ns |
| d _{TLH} | Capacitive Loading, Low to High | | 0.06 | | 0.08 | ns/pF |
| d _{THL} | Capacitive Loading, High to Low | | 0.05 | | 0.07 | ns/pF |
| t _{WDO} | Hard-Wired Wide Decode Output | | 0.05 | | 0.07 | ns |

Notes:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.
2. SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note.

A32200DX Timing Characteristics

(Worst-Case Military Conditions)

| Logic Module Propagation Delays | | '-1 Speed | | 'Std' Speed | | |
|--|--|-----------|------|-------------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| Combinatorial Functions | | | | | | |
| t _{PD} | Internal Array Module Delay | | 2.8 | | 3.8 | ns |
| t _{PDD} | Internal Decode Module Delay | | 3.4 | | 4.6 | ns |
| Predicted Module Routing Delays | | | | | | |
| t _{RD1} | FO=1 Routing Delay | | 1.6 | | 2.1 | ns |
| t _{RD2} | FO=2 Routing Delay | | 2.3 | | 3.1 | ns |
| t _{RD3} | FO=3 Routing Delay | | 2.9 | | 3.9 | ns |
| t _{RD4} | FO=4 Routing Delay | | 3.5 | | 4.7 | ns |
| t _{RD5} | FO=8 Routing Delay | | 6.2 | | 8.2 | ns |
| t _{RDD} | Decode-to-Output Routing Delay | | 0.8 | | 1.1 | ns |
| Sequential Timing Characteristics | | | | | | |
| t _{CO} | Flip-Flop Clock-to-Output | | 3.2 | | 4.2 | ns |
| t _{GO} | Latch Gate-to-Output | | 2.8 | | 3.8 | ns |
| t _{SU} | Flip-Flop (Latch) Setup Time | 0.5 | | 0.6 | | ns |
| t _H | Flip-Flop (Latch) Hold Time | 0.0 | | 0.0 | | ns |
| t _{RO} | Flip-Flop (Latch) Reset to Output | | 3.2 | | 4.2 | ns |
| t _{SUENA} | Flip-Flop (Latch) Enable Setup | 0.9 | | 1.2 | | ns |
| t _{HENA} | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | ns |
| t _{WCLKA} | Flip-Flop (Latch) Clock Active Pulse Width | 4.3 | | 5.8 | | ns |
| t _{WASYN} | Flip-Flop (Latch) Asynchronous Pulse Width | 5.7 | | 7.6 | | ns |

A32200DX Timing Characteristics (continued)

(Worst-Case Military Conditions)

| Logic Module Timing | | '-1 Speed | | 'Std' Speed | | |
|-------------------------------------|------------------------------------|-----------|------|-------------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| Synchronous SRAM Operations | | | | | | |
| t_{RC} | Read Cycle Time | 8.8 | | 11.8 | | ns |
| t_{WC} | Write Cycle Time | 8.8 | | 11.8 | | ns |
| t_{RCKHL} | Clock High/Low Time | 4.4 | | 5.9 | | ns |
| t_{RCO} | Data Valid After Clock High/Low | | 4.4 | | 5.9 | ns |
| t_{ADSU} | Address/Data Setup Time | 2.1 | | 2.8 | | ns |
| t_{ADH} | Address/Data Hold Time | 0.0 | | 0.0 | | ns |
| t_{RENSU} | Read Enable Setup | 0.8 | | 1.1 | | ns |
| t_{RENH} | Read Enable Hold | 4.4 | | 5.9 | | ns |
| t_{WENSU} | Write Enable Setup | 3.5 | | 4.7 | | ns |
| t_{WENH} | Write Enable Hold | 0.0 | | 0.0 | | ns |
| t_{BENS} | Block Enable Setup | 3.6 | | 4.8 | | ns |
| t_{BENH} | Block Enable Hold | 0.0 | | 0.0 | | ns |
| Asynchronous SRAM Operations | | | | | | |
| t_{RPD} | Asynchronous Access Time | | 10.6 | | 14.1 | ns |
| t_{RDADV} | Read Address Valid | 11.5 | | 15.3 | | ns |
| t_{ADSU} | Address/Data Setup Time | 2.1 | | 2.8 | | ns |
| t_{ADH} | Address/Data Hold Time | 0.0 | | 0.0 | | ns |
| t_{RENSUA} | Read Enable Setup to Address Valid | 0.8 | | 1.1 | | ns |
| t_{RENHA} | Read Enable Hold | 4.4 | | 5.9 | | ns |
| t_{WENSU} | Write Enable Setup | 3.5 | | 4.7 | | ns |
| t_{WENH} | Write Enable Hold | 0.0 | | 0.0 | | ns |
| t_{DOH} | Data Out Hold Time | | 1.6 | | 2.1 | ns |

A32200DX Timing Characteristics (continued)

(Worst-Case Military Conditions)

| Input Module Propagation Delays | | | '-1' Speed | | 'Std' Speed | | |
|---------------------------------------|---|--------|------------|------|-------------|------|-------|
| Parameter | Description | | Min. | Max. | Min. | Max. | Units |
| t _{INPY} | Input Data Pad to Y | | | 1.9 | | 2.6 | ns |
| t _{INGO} | Input Latch Gate-to-Output ¹ | | | 4.6 | | 6.0 | ns |
| t _{INH} | Input Latch Hold ¹ | | 0.0 | | 0.0 | | ns |
| t _{INSU} | Input Latch Setup ¹ | | 0.7 | | 0.9 | | ns |
| t _{ILA} | Latch Active Pulse Width ¹ | | 6.1 | | 8.1 | | ns |
| Input Module Predicted Routing Delays | | | | | | | |
| t _{IRD1} | FO=1 Routing Delay | | | 2.6 | | 3.5 | ns |
| t _{IRD2} | FO=2 Routing Delay | | | 3.4 | | 4.6 | ns |
| t _{IRD3} | FO=3 Routing Delay | | | 4.6 | | 6.1 | ns |
| t _{IRD4} | FO=4 Routing Delay | | | 5.4 | | 7.2 | ns |
| t _{IRD5} | FO=8 Routing Delay | | | 7.0 | | 9.3 | ns |
| Global Clock Network | | | | | | | |
| t _{CKH} | Input Low to High | FO=32 | | 7.3 | | 9.8 | ns |
| | | FO=635 | | 8.5 | | 11.3 | ns |
| t _{CKL} | Input High to Low | FO=32 | | 7.2 | | 9.6 | ns |
| | | FO=635 | | 9.3 | | 12.5 | ns |
| t _{PWH} | Minimum Pulse Width High | FO=32 | 3.2 | | 4.3 | | ns |
| | | FO=635 | 3.9 | | 5.2 | | ns |
| t _{PWL} | Minimum Pulse Width Low | FO=32 | 3.2 | | 4.3 | | ns |
| | | FO=635 | 3.9 | | 5.2 | | ns |
| t _{CKSW} | Maximum Skew | FO=32 | | 1.8 | | 2.4 | ns |
| | | FO=635 | | 1.8 | | 2.4 | ns |
| t _{SUEXT} | Input Latch External Setup | FO=32 | 0.0 | | 0.0 | | ns |
| | | FO=635 | 0.0 | | 0.0 | | ns |
| t _{HEXT} | Input Latch External Hold | FO=32 | 3.0 | | 4.0 | | ns |
| | | FO=635 | 3.8 | | 5.1 | | ns |
| t _P | Minimum Period (1/f _{max}) | FO=32 | 5.8 | | 7.7 | | ns |
| | | FO=635 | 6.8 | | 9.1 | | ns |
| f _{HMAX} | Maximum Datapath Frequency | FO=32 | | 172 | | 130 | MHz |
| | | FO=635 | | 147 | | 110 | MHz |

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.

A32200DX Timing Characteristics (continued)

(Worst-Case Military Conditions)

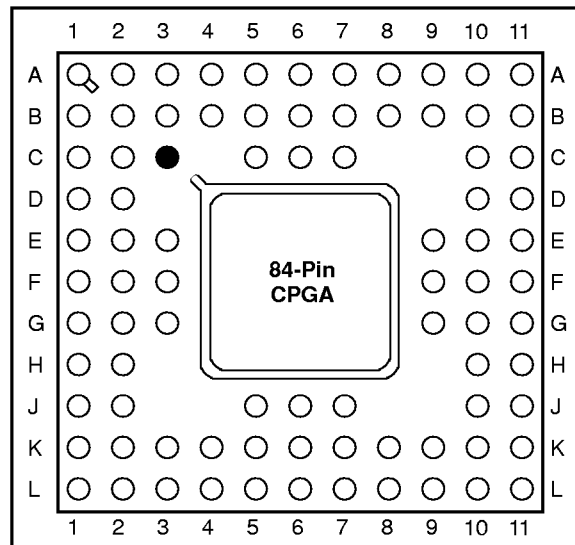
| Output Module Timing | | '-1' Speed | | 'Std' Speed | | |
|--|---|------------|------|-------------|------|-------|
| Parameter | Description | Min. | Max. | Min. | Max. | Units |
| TTL Output Module Timing¹ | | | | | | |
| t _{DLH} | Data to Pad High | | 5.1 | | 6.8 | ns |
| t _{DHL} | Data to Pad Low | | 6.3 | | 8.3 | ns |
| t _{ENZH} | Enable Pad Z to High | | 6.6 | | 8.8 | ns |
| t _{ENZL} | Enable Pad Z to Low | | 7.1 | | 9.5 | ns |
| t _{ENHZ} | Enable Pad High to Z | | 11.5 | | 15.3 | ns |
| t _{ENLZ} | Enable Pad Low to Z | | 11.5 | | 15.3 | ns |
| t _{GLH} | G to Pad High | | 11.5 | | 15.3 | ns |
| t _{GHL} | G to Pad Low | | 12.3 | | 16.5 | ns |
| t _{LSU} | I/O Latch Output Setup | 0.4 | | 0.5 | | ns |
| t _{LH} | I/O Latch Output Hold | 0.0 | | 0.0 | | ns |
| t _{LCO} | I/O Latch Clock-Out (Pad-to-Pad) 32 I/O | | 11.5 | | 15.4 | ns |
| t _{ACO} | Array Latch Clock-Out (Pad-to-Pad) 32 I/O | | 16.3 | | 21.7 | ns |
| d _{TLH} | Capacitive Loading, Low to High | | 0.04 | | 0.06 | ns/pF |
| d _{THL} | Capacitive Loading, High to Low | | 0.06 | | 0.08 | ns/pF |
| t _{WDO} | Hard-Wired Wide Decode Output | | 0.05 | | 0.07 | ns |
| CMOS Output Module Timing¹ | | | | | | |
| t _{DLH} | Data to Pad High | | 5.1 | | 6.8 | ns |
| t _{DHL} | Data to Pad Low | | 6.3 | | 8.3 | ns |
| t _{ENZH} | Enable Pad Z to High | | 6.6 | | 8.8 | ns |
| t _{ENZL} | Enable Pad Z to Low | | 7.1 | | 9.5 | ns |
| t _{ENHZ} | Enable Pad High to Z | | 11.5 | | 15.3 | ns |
| t _{ENLZ} | Enable Pad Low to Z | | 11.5 | | 15.3 | ns |
| t _{GLH} | G to Pad High | | 11.5 | | 15.3 | ns |
| t _{GHL} | G to Pad Low | | 12.3 | | 16.5 | ns |
| t _{LSU} | I/O Latch Setup | 0.4 | | 0.5 | | ns |
| t _{LH} | I/O Latch Hold | 0.0 | | 0.0 | | ns |
| t _{LCO} | I/O Latch Clock-Out (Pad-to-Pad) 32 I/O | | 13.7 | | 18.2 | ns |
| t _{ACO} | Array Latch Clock-Out (Pad-to-Pad) 32 I/O | | 19.2 | | 25.6 | ns |
| d _{TLH} | Capacitive Loading, Low to High | | 0.06 | | 0.08 | ns/pF |
| d _{THL} | Capacitive Loading, High to Low | | 0.05 | | 0.07 | ns/pF |
| t _{WDO} | Hard-Wired Wide Decode Output | | 0.05 | | 0.07 | ns |

Notes:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.
2. SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note.

Package Pin Assignments

84-Pin CPGA (Top View)



● Orientation Pin (C3)

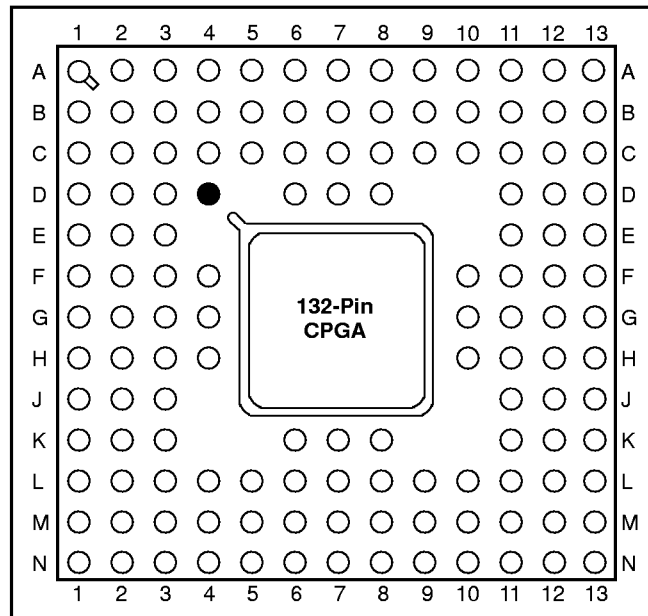
| Function | A1010B Pin Number | A1020B Pin Number |
|---------------------|--|-----------------------------|
| CLK or I/O | F9 | F9 |
| DCLK or I/O | C10 | C10 |
| GND | B7, E2, E3, F10, G10, K5 | B7, E2, E3, F10, G10, K5 |
| MODE | E11 | E11 |
| N/C (No Connection) | B1, B2, C1, C2, C11, D10, D11, J2, J10, K1, K10, K11, L1 | B2 |
| PRA or I/O | A11 | A11 |
| PRB or I/O | B10 | B10 |
| SDI or I/O | B11 | B11 |
| V _{CC} | B5, E9, E10, F1, G2, K2, K7 | B5, E9, E10, F1, G2, K2, K7 |

Notes:

1. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.*
2. *Unused I/O pins are designated as outputs by ALS and are driven low.*
3. *All unassigned pins are available for use as I/Os*

Package Pin Assignments (continued)

132-Pin CPGA (Top View)



● Orientation Pin

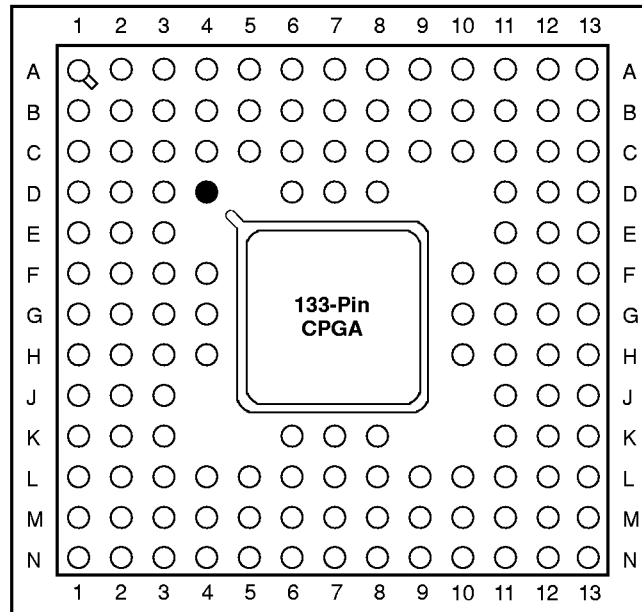
| Function | A1240A Pin Number |
|-----------------|---|
| CLKA or I/O | B7 |
| CLKB or I/O | B6 |
| DCLK or I/O | C3 |
| GND | B5, B9, C5, C9, E3, E11, E12, F4, H13, J2, J3, J11, K12, L5, L9, M9 |
| MODE | A1 |
| PRA or I/O | B8 |
| PRB or I/O | C6 |
| SDI or I/O | B12 |
| V _{CC} | C7, D7, G2, G3, G4, G10, G11, G12, G13, K7, L7 |

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.

Package Pin Assignments (continued)

133-Pin CPGA (Top View)



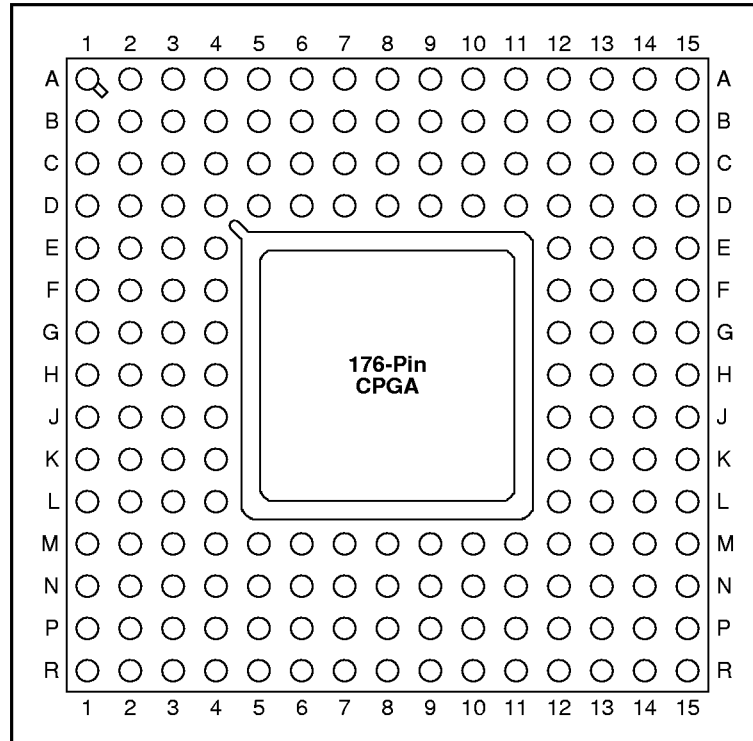
| Function | A1425A Pin Number |
|-----------------|--|
| CLKA or I/O | D7 |
| CLKB or I/O | B6 |
| DCLK or I/O | D4 |
| GND | A2, C3, C7, C11, C12, F10, G3, G11, L3, L7, L11, M3, N12 |
| HCLKA or I/O | K7 |
| IOCLK or I/O | C10 |
| IOPCL or I/O | L10 |
| MODE | E3 |
| NC | A1, A7, A13, G1, G13, N1, N7, N13 |
| PRA or I/O | A6 |
| PRB or I/O | L6 |
| SDI or I/O | C2 |
| V _{CC} | B2, B7, B12, E11, G2, G12, J2, J12, M2, M7, M12 |

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.

Package Pin Assignments (continued)

176-Pin CPGA (Top View)



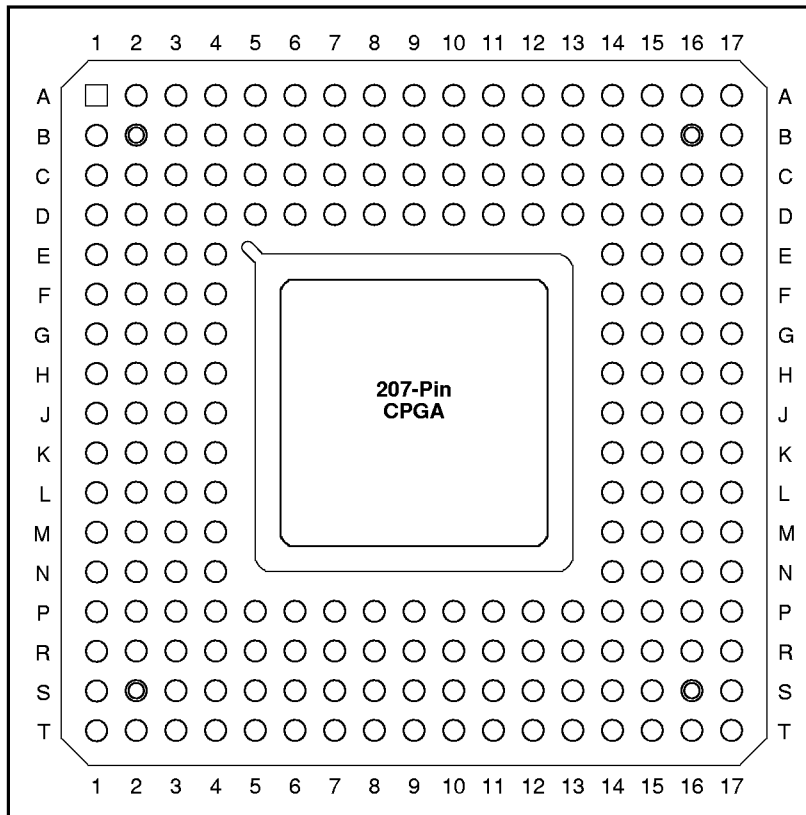
| Function | A1280A, A1280XL Pin Number |
|-----------------|--|
| CLKA or I/O | A9 |
| CLKB or I/O | B8 |
| DCLK or I/O | B3 |
| GND | C8, D4, D6, D10, D12, E4, E12, F12, G4, H4, H12, J12, J13, K4, K12, L4, M4, M6, M8, M10, M12 |
| MODE | C3 |
| PRA or I/O | C9 |
| PRB or I/O | D7 |
| SDI or I/O | B14 |
| V _{CC} | D5, D8, D11, F4, G12, H2, H3, H13, H14, J4, J14, M5, M11, N8 |

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.

Package Pin Assignments (continued)

207-Pin CPGA (Top View)



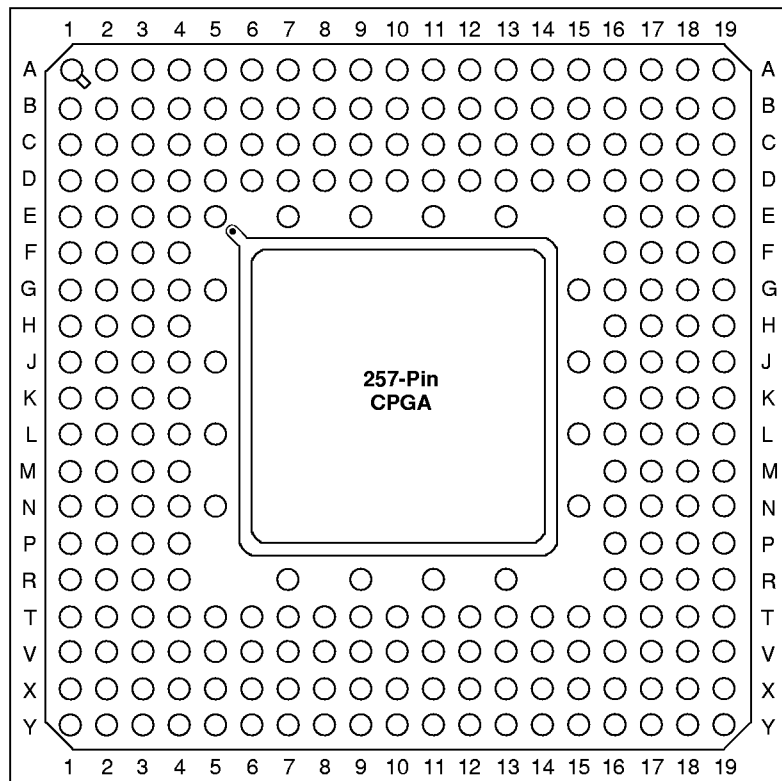
| Function | A1460A Pin Number |
|-----------------|--|
| CLKA or I/O | K1 |
| CLKB or I/O | J3 |
| DCLK or I/O | E4 |
| GND | C15, D4, D5, D9, D14, J4, J14, P3, P4, P7, P9, P14, R15 |
| HCKL or I/O | J15 |
| IOCLK or I/O | P5 |
| IOPCL or I/O | N14 |
| MODE | D7 |
| NC | A1, A2, A16, A17, B1, B17, C1, C2, S1, S3, S17, T1, T2, T16, T17 |
| PRA OR I/O | H1 |
| PRB or I/O | K16 |
| SDI or I/O | C3 |
| V _{CC} | B2, B9, B16, D11, J2, J16, P12, S2, S9, S16, T5 |

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.

Package Pin Assignments (continued)

257-Pin CPGA (Top View)



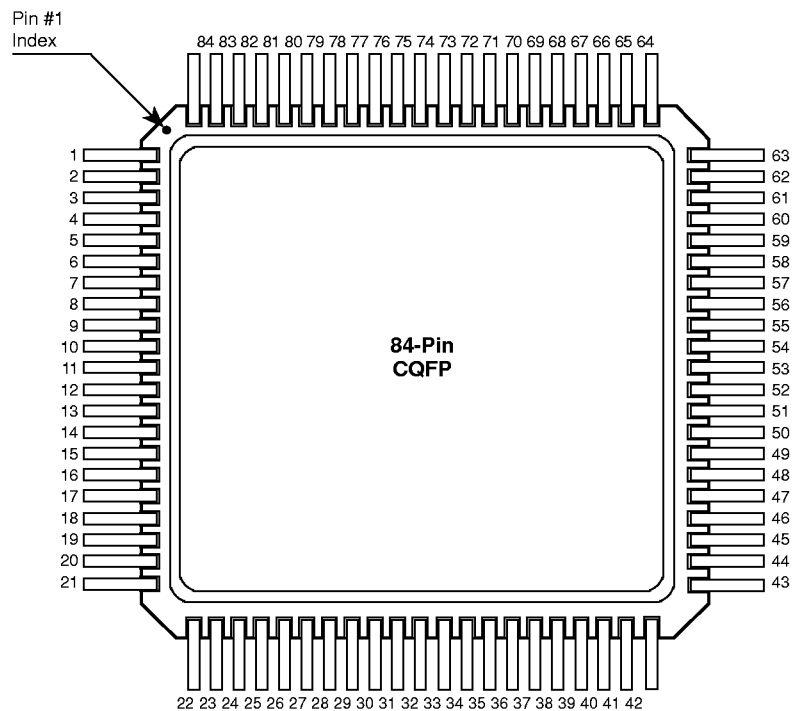
| Function | A14100A Pin Number |
|-----------------|---|
| CLKA or I/O | L4 |
| CLKB or I/O | L5 |
| DCLK or I/O | E4 |
| GND | B16, C4, D4, D10, D16, E11, J5, K4, K16, L15, R4, T4, T10, T16, T17, X7 |
| HCLK or I/O | J16 |
| IOCLK or I/O | T5 |
| IOPCL or I/O | R16 |
| MODE | A5 |
| NC | E5 |
| PRA OR I/O | J1 |
| PRB or I/O | J17 |
| SDI or I/O | B4 |
| V _{CC} | C3, C10, C13, C17, K3, K17, V3, V7, V10, V17, X14 |

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.

Package Pin Assignments (continued)

84-Pin CQFP (Top View)



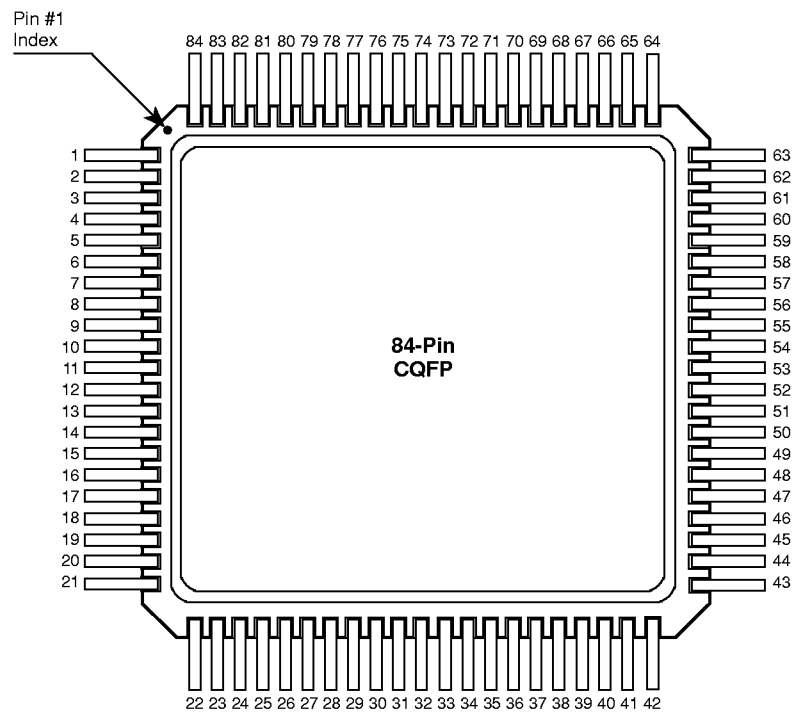
| Function | A1020B Pin Number |
|---------------------|----------------------------|
| CLKA or I/O | 53 |
| DCLK or I/O | 62 |
| GND | 7, 8, 29, 49, 50, 71 |
| MODE | 55 |
| N/C (No Connection) | 1 |
| PRA or I/O | 63 |
| PRB or I/O | 64 |
| SDI or I/O | 61 |
| V _{CC} | 14, 15, 22, 35, 56, 57, 77 |

Notes:

1. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.
2. Unused I/O pins are designated as outputs by ALS and are driven low.
3. All unassigned pins are available for use as I/Os

Package Pin Assignments (continued)

84-Pin CQFP (Top View)

**Notes:**

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.

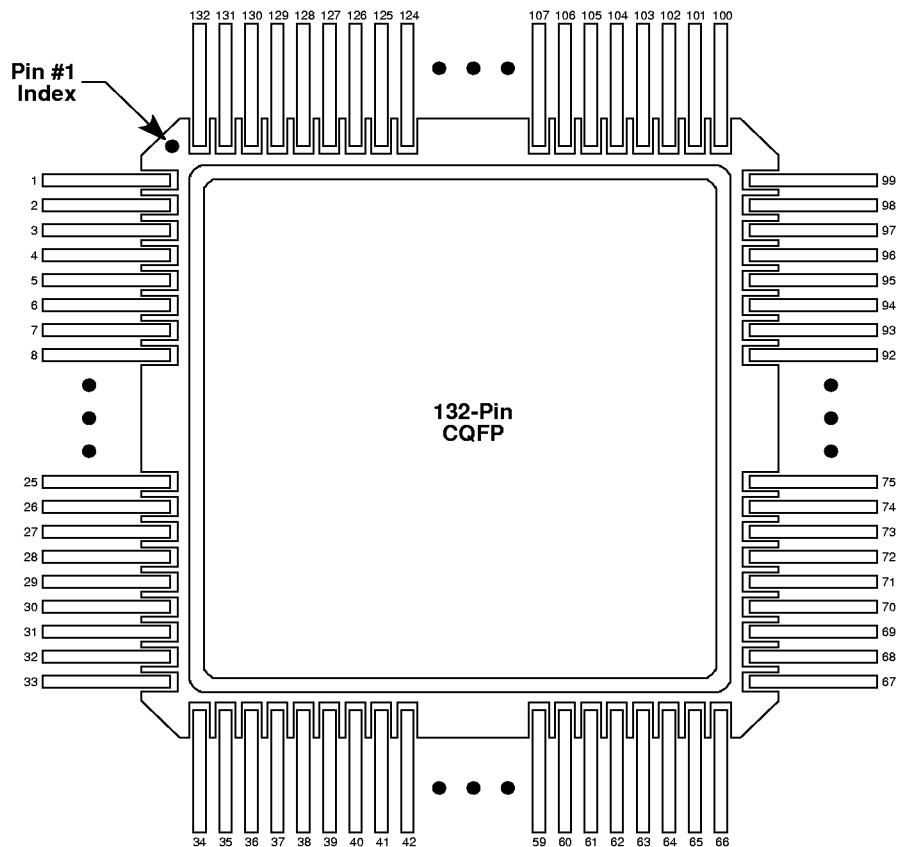
84-Pin CQFP (continued)

| Pin Number | A32100DX Function |
|------------|-------------------|
| 1 | GND |
| 2 | MODE |
| 7 | V _{CC} |
| 10 | GND |
| 11 | V _{CC} |
| 12 | V _{CC} |
| 17 | GND |
| 22 | GND |
| 25 | I/O (WD) |
| 26 | I/O (WD) |
| 28 | QCLKA, I/O |
| 29 | GND |
| 30 | I/O (WD) |
| 32 | GND |
| 33 | V _{CC} |
| 34 | I/O (WD) |
| 35 | I/O (WD) |
| 36 | QCLKB, I/O |
| 37 | I/O (WD) |
| 38 | GND |
| 39 | I/O (WD) |
| 40 | I/O (WD) |
| 41 | I/O (WD) |
| 42 | SDO, I/O |
| 43 | GND |
| 50 | GND |
| 51 | TCK, I/O |
| 52 | GND |

| Pin Number | A32100DX Function |
|------------|-------------------|
| 53 | V _{CC} |
| 54 | V _{CC} |
| 55 | V _{CC} |
| 56 | V _{CC} |
| 59 | GND |
| 63 | GND |
| 64 | SDI, I/O |
| 65 | I/O (WD) |
| 66 | I/O (WD) |
| 67 | I/O (WD) |
| 68 | I/O (WD) |
| 69 | QCLKD, I/O |
| 70 | I/O (WD) |
| 71 | I/O (WD) |
| 72 | PRA, I/O |
| 73 | CLKA, I/O |
| 74 | V _{CC} |
| 75 | GND |
| 76 | CLKB, I/O |
| 77 | PRB, I/O |
| 78 | I/O (WD) |
| 79 | I/O (WD) |
| 80 | QCLKC, I/O |
| 81 | GND |
| 82 | I/O (WD) |
| 83 | I/O (WD) |
| 84 | DCLK, I/O |

Package Pin Assignments (continued)

132-Pin CQFP (Top View)



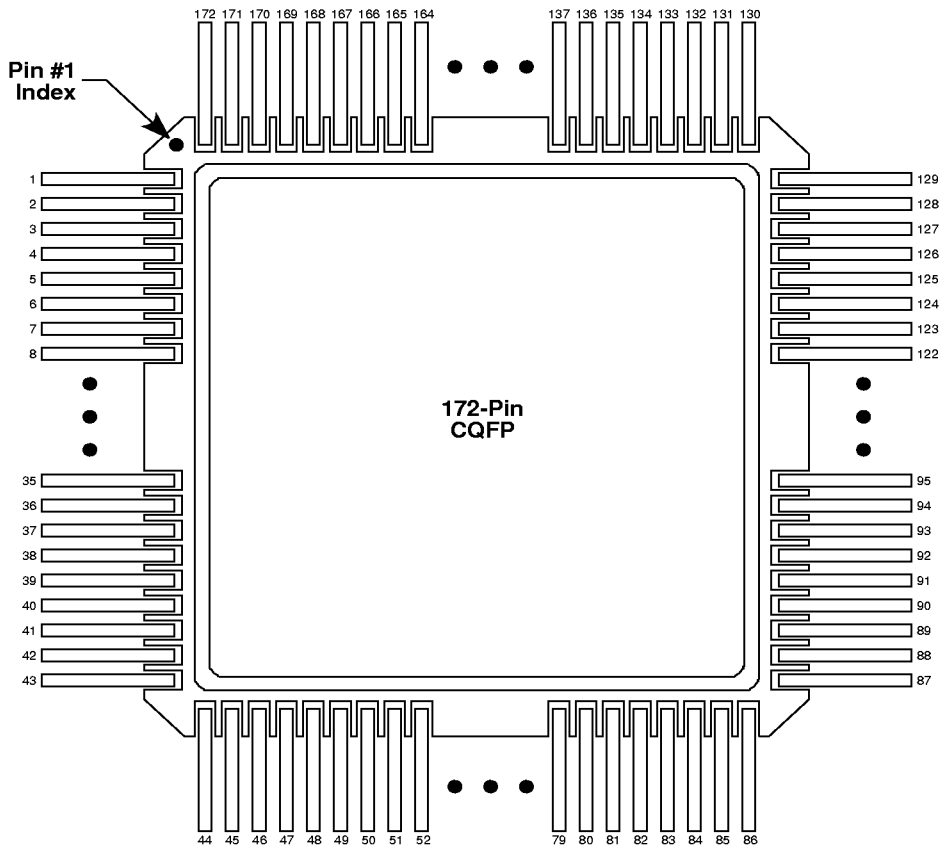
| Function | A1425A Pin Number |
|-----------------|--|
| CLKA or I/O | 116 |
| CLKB or I/O | 117 |
| DCLK or I/O | 131 |
| GND | 2, 10, 26, 36, 42, 58, 65, 74, 90, 92, 101, 106, 122 |
| HCLK or I/O | 50 |
| IOCLK or I/O | 98 |
| IOPCL or I/O | 64 |
| MODE | 9 |
| NC | 1, 34, 66, 67, 99, 100, 132 |
| PRA or I/O | 118 |
| PRB or I/O | 48 |
| SDI or I/O | 3 |
| V _{CC} | 11, 22, 27, 43, 59, 75, 78, 89, 91, 107, 123 |

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.

Package Pin Assignments (continued)

172-Pin CQFP (Top View)



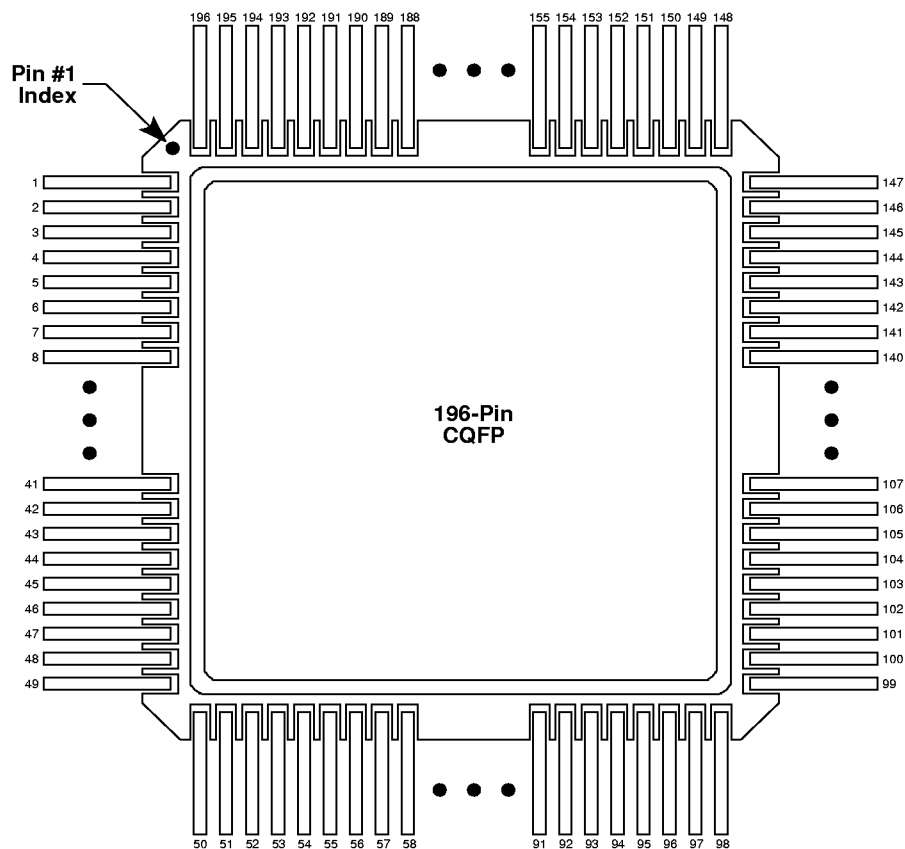
| Function | A1280A, A1280XL Pin Number |
|-----------------|---|
| CLKA or I/O | 150 |
| CLKB or I/O | 154 |
| DCLK or I/O | 171 |
| GND | 7, 17, 22, 32, 37, 55, 65, 75, 98, 103, 106, 108, 118, 123, 141, 152, 161 |
| MODE | 1 |
| PRA or I/O | 148 |
| PRB or I/O | 156 |
| SDI or I/O | 131 |
| V _{CC} | 12, 23, 24, 27, 66, 80, 107, 109, 110, 113, 136, 151, 166 |

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.

Package Pin Assignments (continued)

196-Pin CQFP (Top View)



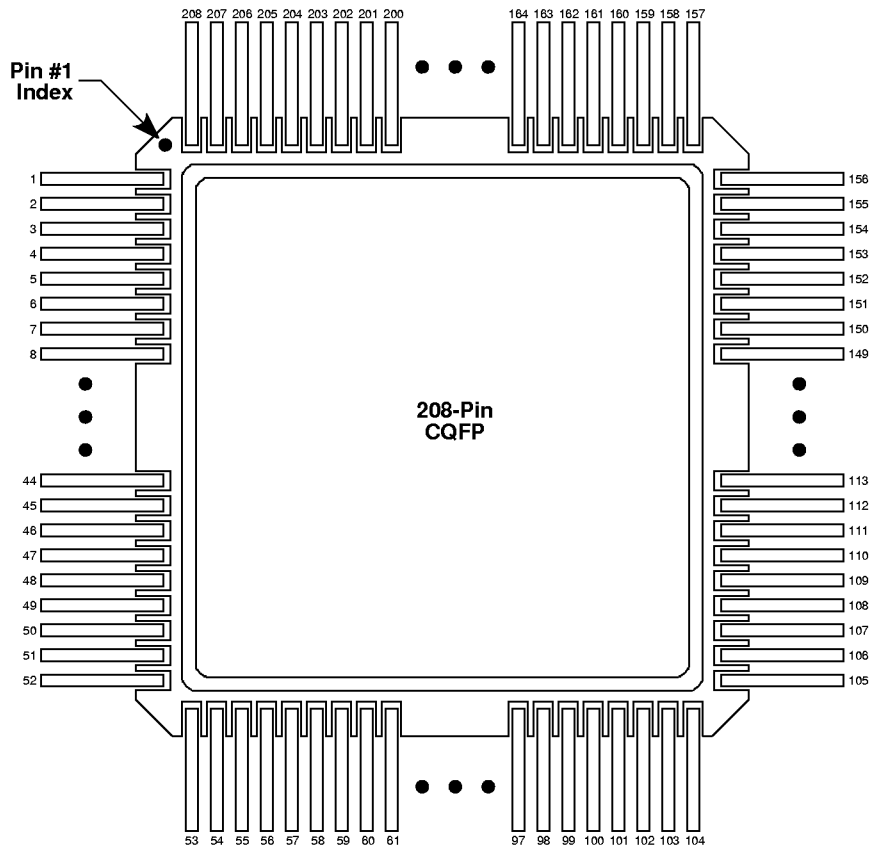
| Function | A1460A Pin Number |
|-----------------|---|
| CLKA or I/O | 172 |
| CLKB or I/O | 173 |
| DCLK or I/O | 196 |
| GND | 1, 13, 37, 51, 52, 64, 86, 98, 101, 112, 138, 139, 149, 162, 183, 193 |
| HCLK or I/O | 77 |
| IOCLK or I/O | 148 |
| IOPCL or I/O | 100 |
| MODE | 11 |
| PRA or I/O | 174 |
| PRB or I/O | 75 |
| SDI or I/O | 2 |
| V _{CC} | 12, 38, 39, 59, 94, 110, 111, 137, 140, 155, 189 |

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.

Package Pin Assignments (continued)

208-Pin CQFP (Top View)



Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE should be terminated to GND through a 10K resistor to enable Action probe usage, otherwise it can be terminated directly to GND.

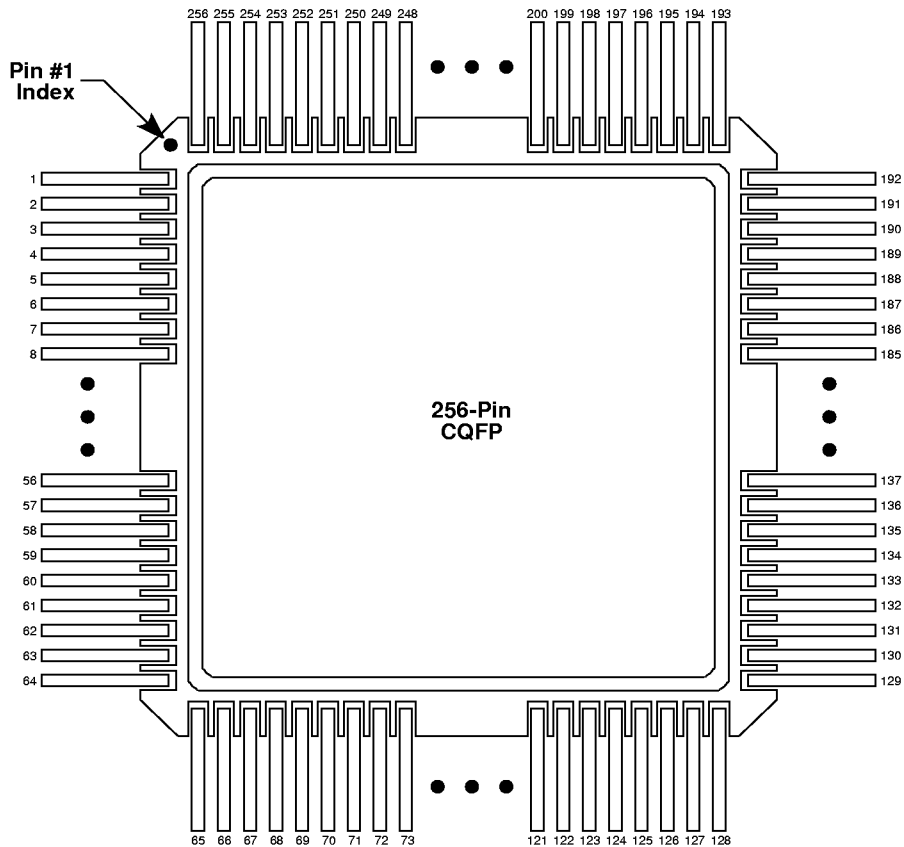
208-Pin CQFP (continued)

| Pin Number | A32100DX Function |
|------------|----------------------|
| 1 | GND |
| 2 | V _{CC} |
| 3 | MODE |
| 17 | V _{CC} |
| 22 | GND |
| 27 | GND |
| 28 | V _{CC} |
| 29 | V _{CC} |
| 32 | V _{CC} |
| 52 | GND |
| 53 | GND |
| 54 | TMS, I/O |
| 55 | TDI, I/O |
| 57 | I/O (WD) |
| 58 | I/O (WD) |
| 60 | V _{CC} |
| 65 | QCLKA, I/O |
| 66 | I/O (WD) |
| 67 | I/O (WD) |
| 70 | I/O (WD) |
| 71 | I/O (WD) |
| 78 | GND |
| 79 | V _{CC} |
| 80 | V _{CC} |
| 85 | I/O (WD) |
| 86 | I/O (WD) |
| 91 | QCLKB, I/O |
| 93 | I/O (WD) |
| 94 | I/O (WD) |
| 98 | V _{CC} |
| 100 | I/O (WD) |
| 101 | I/O (WD) |
| 103 | SDO, I/O |
| 105 | GND |
| 106 | V _{CC} |

| Pin Number | A32100DX Function |
|------------|----------------------|
| 126 | GND |
| 128 | TCK, I/O |
| 129 | GND |
| 130 | V _{CC} |
| 131 | GND |
| 132 | V _{CC} |
| 133 | V _{CC} |
| 136 | V _{CC} |
| 150 | GND |
| 157 | GND |
| 159 | SDI, I/O |
| 161 | I/O (WD) |
| 162 | I/O (WD) |
| 164 | V _{CC} |
| 168 | I/O (WD) |
| 169 | I/O (WD) |
| 171 | QCLKD, I/O |
| 176 | I/O (WD) |
| 177 | I/O (WD) |
| 178 | PRA, I/O |
| 180 | CLKA, I/O |
| 182 | V _{CC} |
| 183 | V _{CC} |
| 184 | GND |
| 186 | CLKB, I/O |
| 188 | PRB, I/O |
| 190 | I/O (WD) |
| 191 | I/O (WD) |
| 194 | I/O (WD) |
| 195 | I/O (WD) |
| 196 | QCLKC, I/O |
| 202 | V _{CC} |
| 203 | I/O (WD) |
| 204 | I/O (WD) |
| 207 | DCLK, I/O |

Package Pin Assignments (continued)

256-Pin CQFP (Top View)



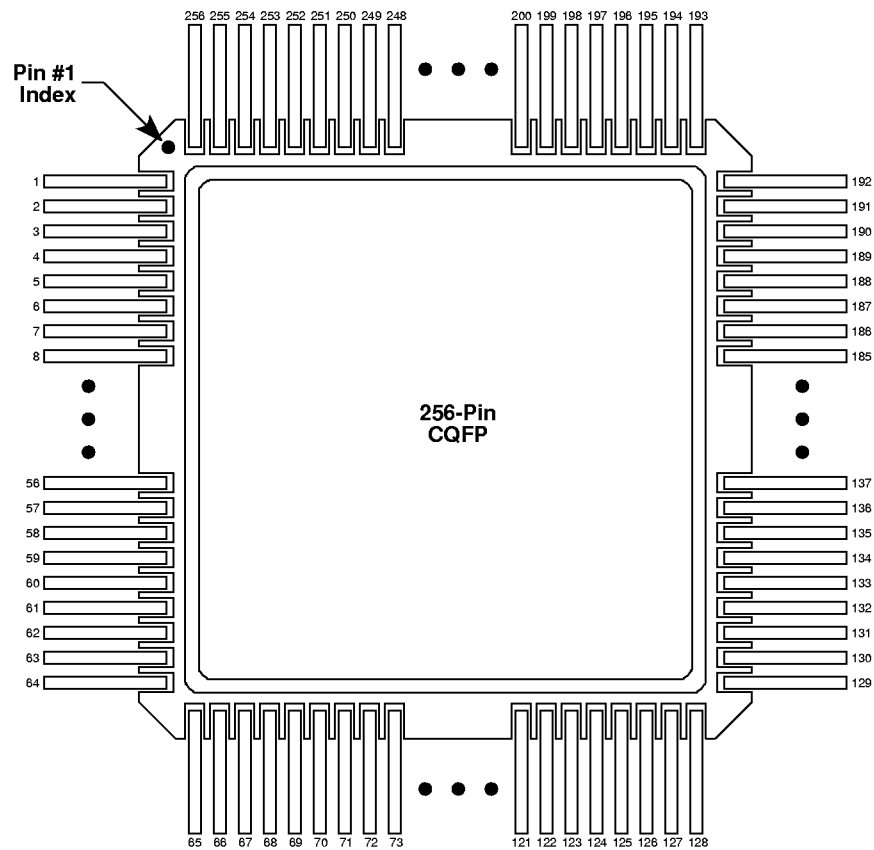
| Function | A14100A Pin Number |
|-----------------|---|
| CLKA or I/O | 219 |
| CLKB or I/O | 220 |
| DCLK or I/O | 256 |
| GND | 1, 29, 31, 59, 91, 93, 110, 128, 158, 160, 175, 176, 189, 222, 224, 240 |
| HCLK or I/O | 96 |
| IOCLK or I/O | 188 |
| IOPCL or I/O | 127 |
| MODE | 11 |
| PRA or I/O | 225 |
| PRB or I/O | 90 |
| SDI or I/O | 2 |
| V _{CC} | 28, 30, 46, 92, 94, 141, 159, 161, 174, 221, 223 |

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.

Package Pin Assignments (continued)

256-Pin CQFP (Top View)

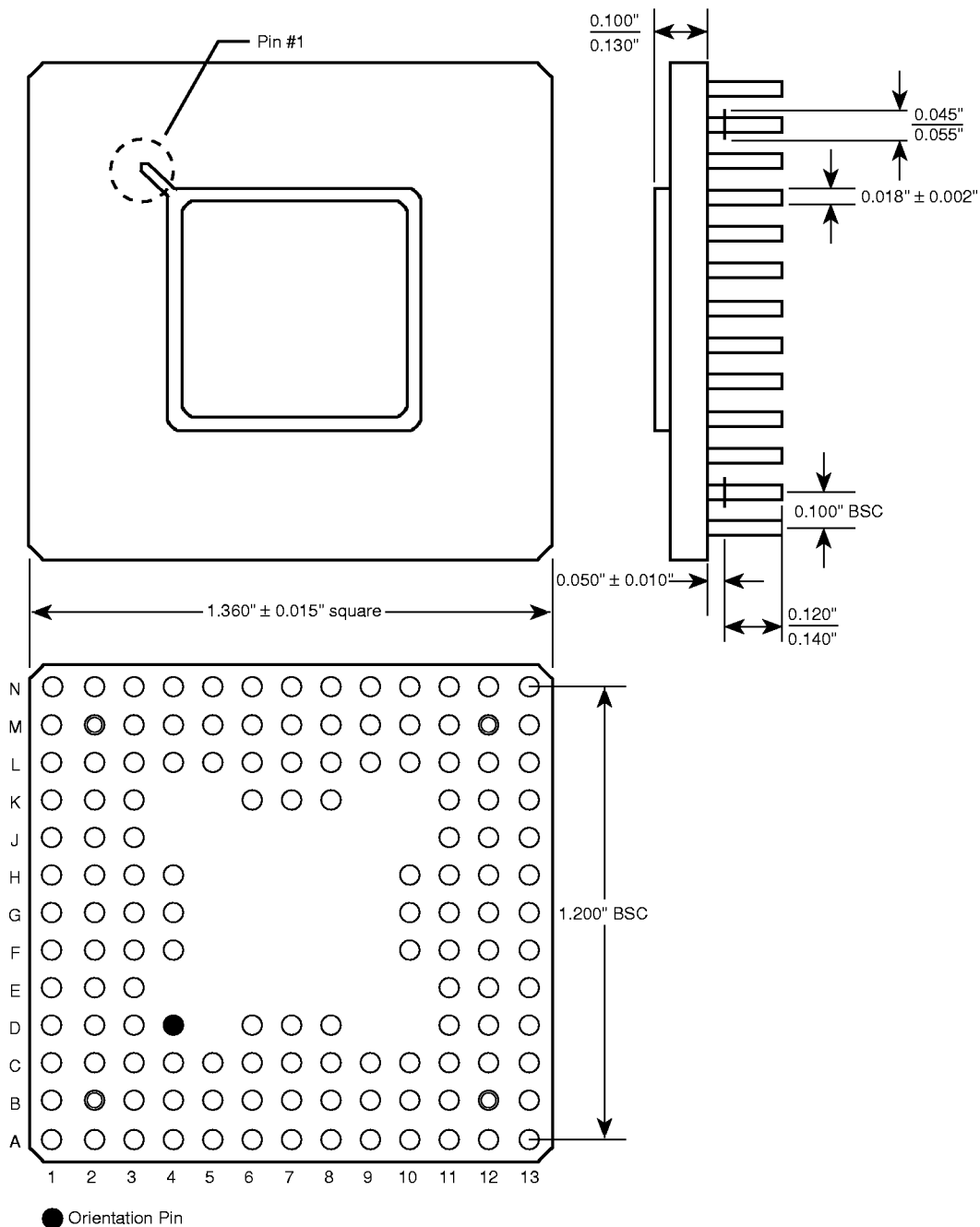
**Notes:**

1. NC: Denotes No Connection
2. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.

256-Pin CQFP (continued)

| Pin Number | A32200DX Function | Pin Number | A32200DX Function | Pin Number | A32200DX Function |
|------------|-------------------|------------|-------------------|------------|-------------------|
| 1 | NC | 95 | VCC | 191 | NC |
| 2 | GND | 96 | VCC | 192 | NC |
| 3 | I/O | 97 | GND | 193 | NC |
| 10 | GND | 98 | GND | 195 | DCLK, I/O |
| 11 | I/O | 105 | I/O (WD) | 198 | I/O |
| 12 | I/O | 106 | I/O (WD) | 199 | I/O (WD) |
| 26 | VCC | 109 | I/O (WD) | 200 | I/O (WD) |
| 29 | VCC | 110 | I/O (WD) | 201 | VCC |
| 30 | VCC | 111 | I/O | 206 | GND |
| 31 | GND | 112 | QCLKA, I/O | 207 | I/O |
| 32 | VCC | 114 | GND | 209 | QCLKC, I/O |
| 33 | GND | 119 | VCC | 211 | I/O (WD) |
| 34 | TCK, I/O | 121 | I/O (WD) | 212 | I/O (WD) |
| 36 | GND | 122 | I/O (WD) | 215 | I/O (WD) |
| 45 | I/O | 124 | I/O | 216 | I/O (WD) |
| 46 | I/O | 125 | TDI, I/O | 218 | PRB, I/O |
| 47 | I/O | 126 | TMS, I/O | 220 | CLKB, I/O |
| 48 | GND | 127 | GND | 222 | GND |
| 60 | VCC | 128 | NC | 223 | GND |
| 61 | GND | 129 | NC | 224 | VCC |
| 62 | GND | 130 | NC | 225 | VCC |
| 63 | NC | 131 | GND | 227 | CLKA, I/O |
| 64 | NC | 138 | I/O | 228 | I/O |
| 65 | NC | 139 | GND | 229 | PRA, I/O |
| 67 | SDO, I/O | 140 | I/O | 230 | I/O |
| 69 | I/O (WD) | 152 | I/O | 231 | I/O |
| 70 | I/O (WD) | 155 | VCC | 232 | I/O (WD) |
| 72 | VCC | 158 | VCC | 233 | I/O (WD) |
| 76 | I/O (WD) | 159 | VCC | 238 | I/O |
| 77 | GND | 160 | GND | 240 | QCLKD, I/O |
| 78 | I/O (WD) | 165 | GND | 242 | I/O (WD) |
| 80 | QCLKB, I/O | 170 | VCC | 243 | GND |
| 86 | I/O | 171 | I/O | 244 | I/O (WD) |
| 87 | I/O (WD) | 173 | I/O | 248 | VCC |
| 88 | I/O (WD) | 180 | GND | 250 | I/O (WD) |
| 89 | I/O | 185 | I/O | 251 | I/O (WD) |
| 92 | I/O | 188 | MODE | 253 | SDI, I/O |
| 93 | I/O | 189 | VCC | 255 | GND |
| 94 | I/O | 190 | GND | 256 | NC |

Package Mechanical Drawings
 133-Pin Ceramic Pin Grid Array (CPGA)

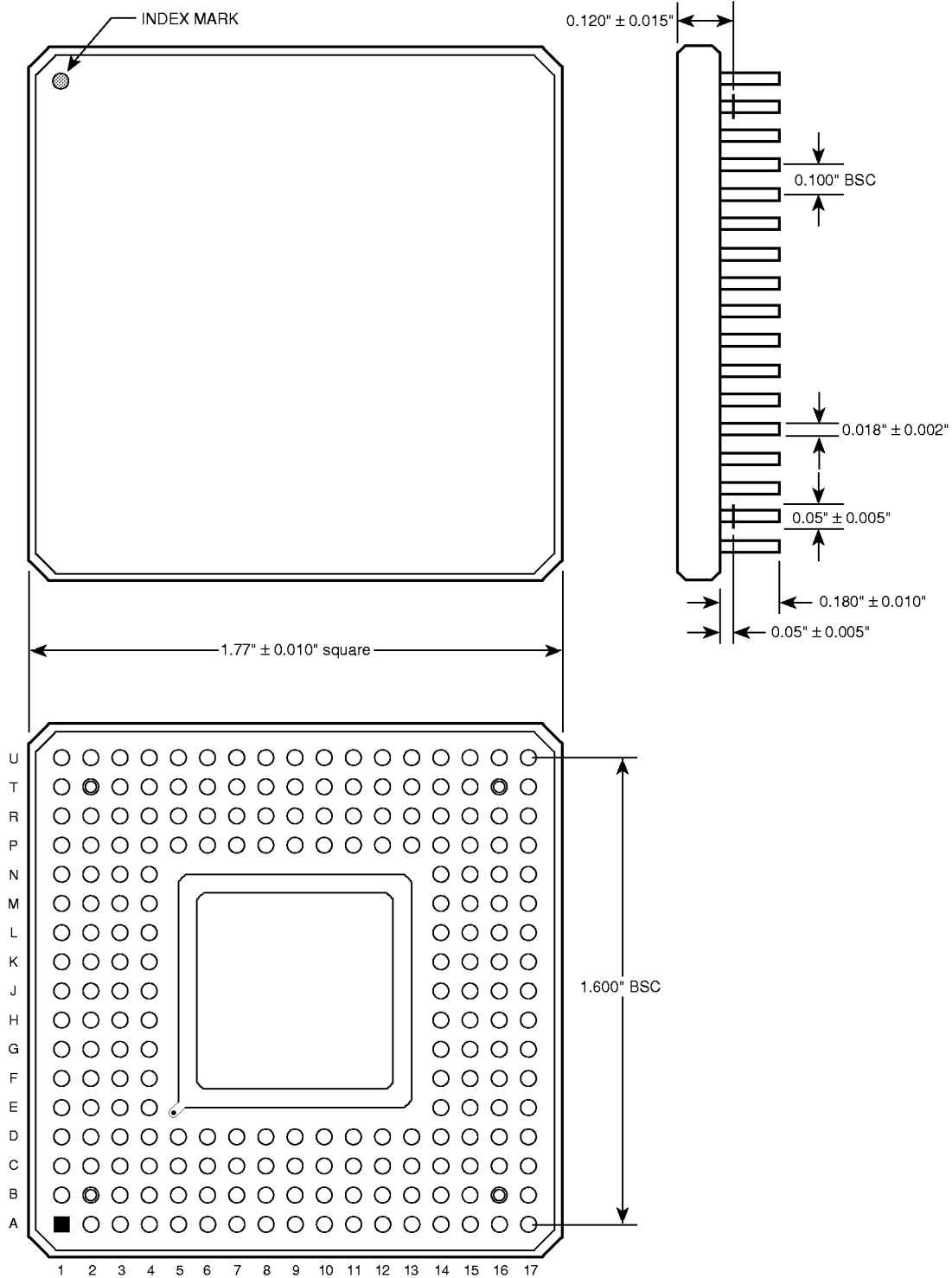


Notes:

1. All dimensions are in inches unless otherwise stated.
2. BSC—Basic Spacing between Centers.

Package Mechanical Drawings (continued)

207-Pin CPGA

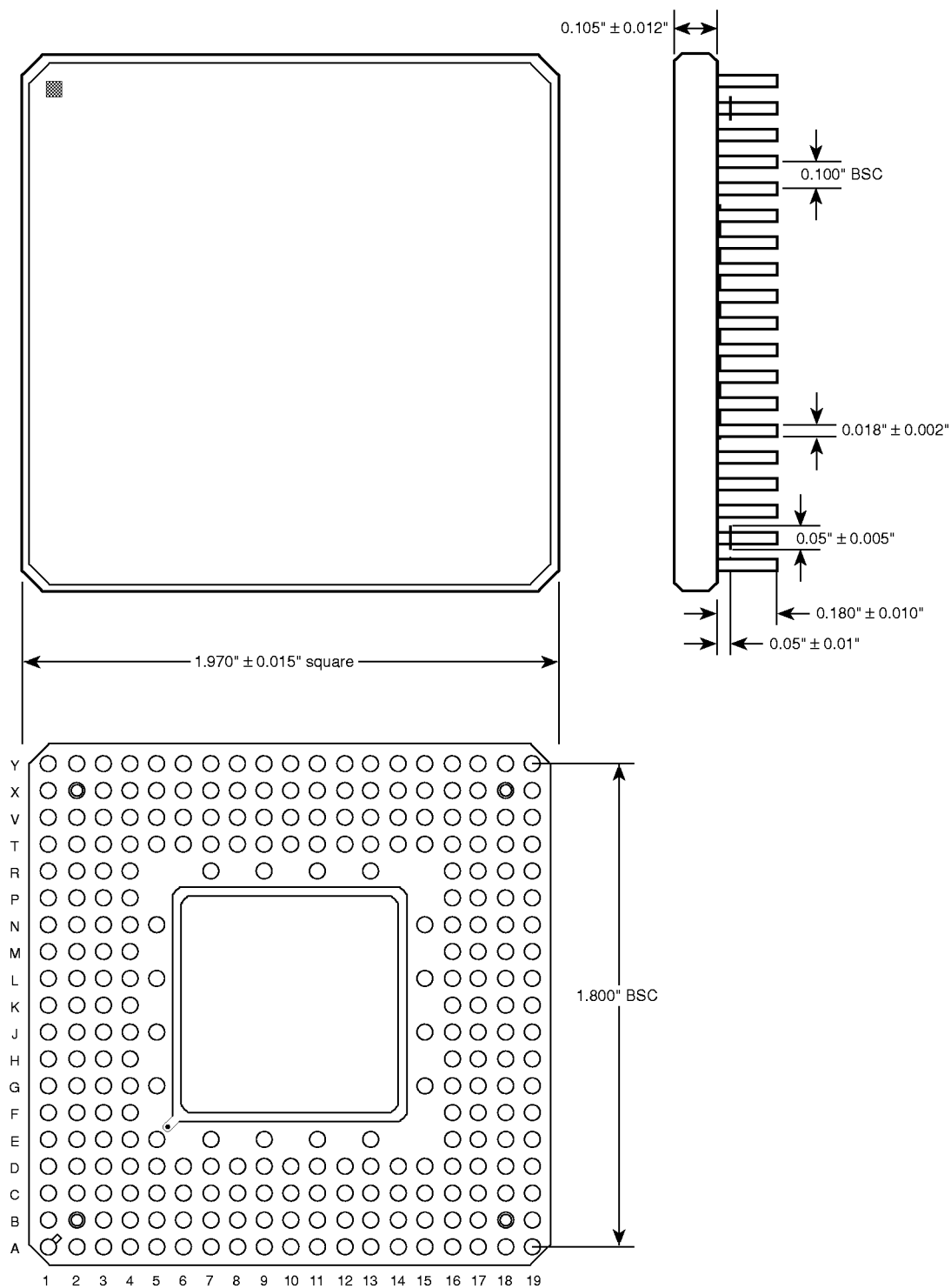


Notes:

1. All dimensions are in inches unless otherwise stated.
2. BSC—Basic Spacing between Centers.

Package Mechanical Drawings (continued)

257-Pin CPGA

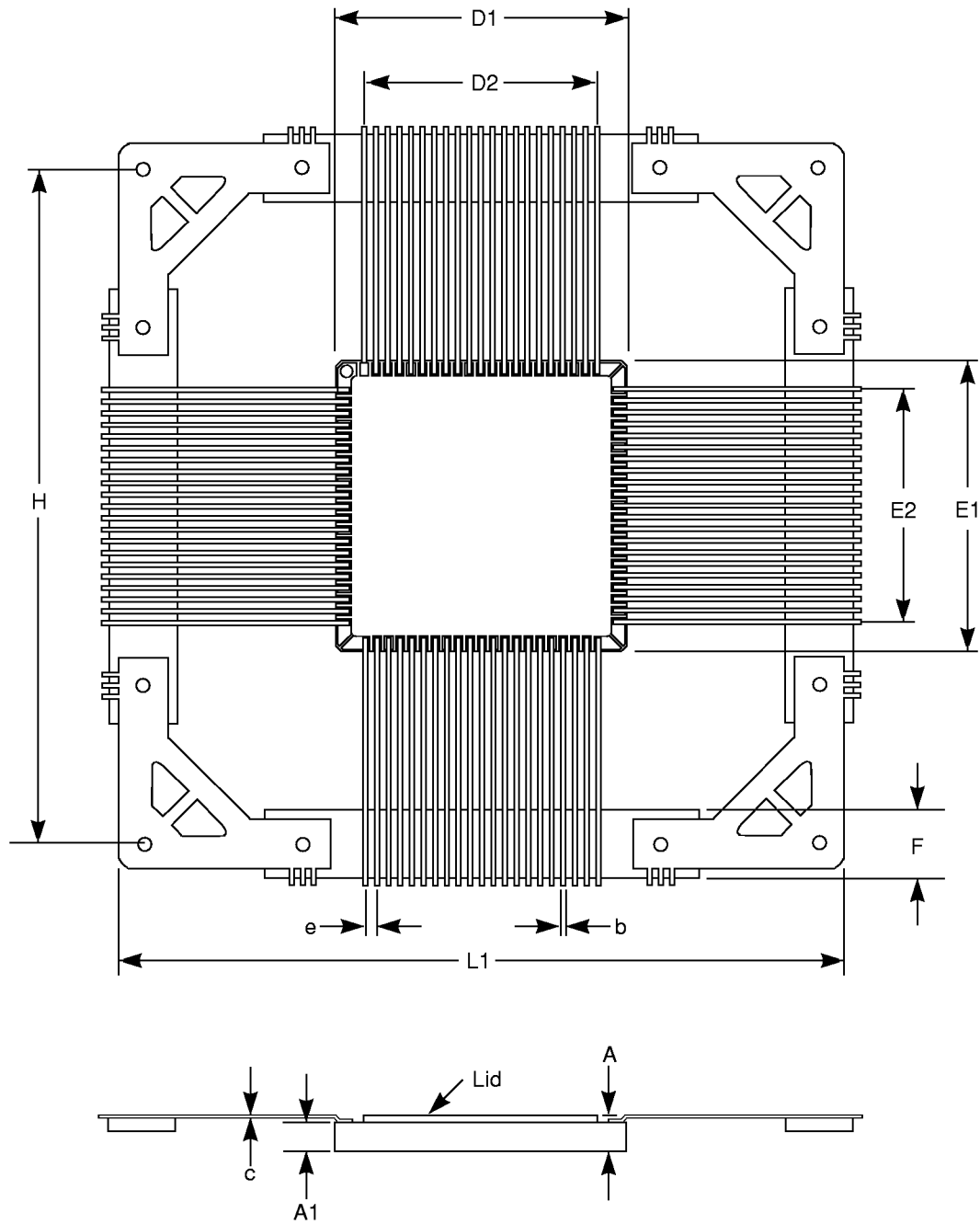


Notes:

1. All dimensions are in inches unless otherwise stated.
2. BSC—Basic Spacing between Centers.

Package Mechanical Drawings (continued)

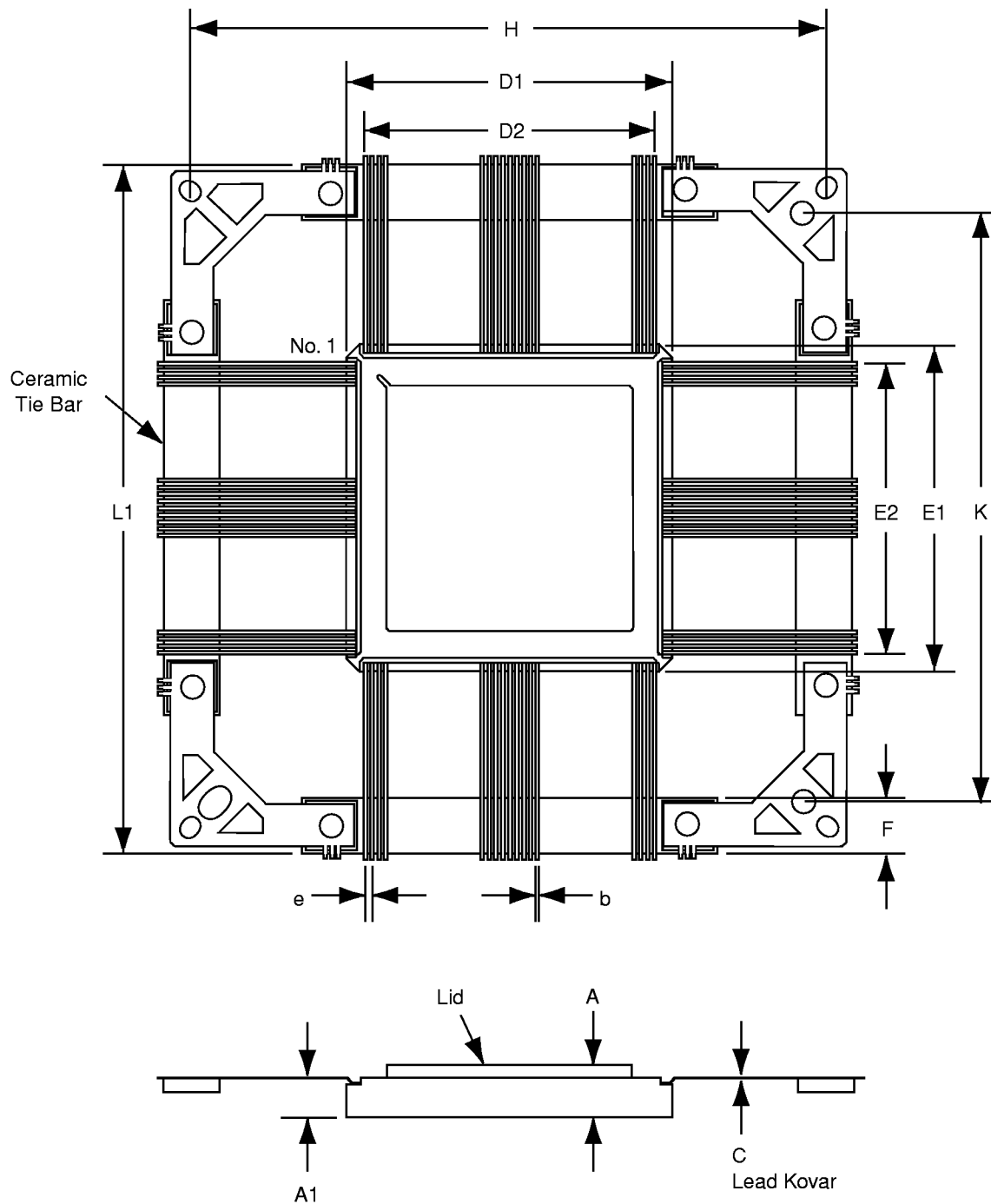
Ceramic Quad Flatpack (84-Pin CQFP)



Notes:

1. Dimensions are in inches.
2. Seal Ring and Lid are connected to Ground.
3. Lead material is Kovar with gold plate over nickel.
4. Packages are shipped unformed with the ceramic tie bar in a test carrier.

Package Mechanical Drawings (continued)
 Ceramic Quad Flatpack (CQFP—Cavity Up)



Notes:

1. All dimensions are in inches except CQ208 and CQ256 which are in millimeters.
2. Outside leadframe holes (from dimension H) are circular for the CQ208 and CQ256.
3. Seal ring and lid are connected to Ground.
4. Lead material is Kovar with minimum 60 micronches gold over nickel.
5. Packages are shipped unformed with the ceramic tie bar.
6. 32200DX - CQ208 has heat sink on the backside.

Ceramic Quad Flatpack (CQFP)

| | CQ84 | | | CQ132 | | | CQ172 | | | CQ196 | | |
|--------|-----------|-------|-------|-----------|-------|-------|-----------|-------|-------|-----------|-------|-------|
| Symbol | Min | Nom. | Max | Min | Nom. | Max | Min | Nom. | Max | Min | Nom. | Max |
| A | 0.070 | 0.090 | 0.100 | 0.094 | 0.105 | 0.116 | 0.094 | 0.105 | 0.116 | 0.094 | 0.105 | 0.116 |
| A1 | 0.060 | 0.075 | 0.080 | 0.080 | 0.090 | 0.100 | 0.080 | 0.090 | 0.100 | 0.080 | 0.090 | 0.100 |
| b | 0.008 | 0.010 | 0.012 | 0.007 | 0.008 | 0.010 | 0.007 | 0.008 | 0.010 | 0.007 | 0.008 | 0.010 |
| c | 0.004 | 0.006 | 0.008 | 0.004 | 0.006 | 0.008 | 0.004 | 0.006 | 0.008 | 0.004 | 0.006 | 0.008 |
| D1/E1 | 0.640 | 0.650 | 0.660 | 0.940 | 0.950 | 0.960 | 1.168 | 1.180 | 1.192 | 1.336 | 1.350 | 1.364 |
| D2/E2 | 0.500 BSC | | | 0.800 BSC | | | 1.050 BSC | | | 1.200 BSC | | |
| e | 0.025 BSC | | | 0.025 BSC | | | 0.025 BSC | | | 0.025 BSC | | |
| F | 0.130 | 0.140 | 0.150 | 0.325 | 0.350 | 0.375 | 0.175 | 0.200 | 0.225 | 0.175 | 0.200 | 0.225 |
| H | 1.460 BSC | | | 2.320 BSC | | | 2.320 BSC | | | 2.320 BSC | | |
| K | — | | | 2.140 BSC | | | 2.140 BSC | | | 2.140 BSC | | |
| L1 | 1.595 | 1.600 | 1.615 | 2.485 | 2.500 | 2.505 | 2.485 | 2.495 | 2.505 | 2.485 | 2.495 | 2.505 |

Note:

1. All dimensions are in inches except CQ208 and CQ256, which is in millimeters.
2. BSC equals Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.

Ceramic Quad Flatpack (CQFP) (continued)

| | CQ208 | | | CQ256 | | |
|--------|-----------|-------|-------|-----------|-------|-------|
| Symbol | Min | Nom. | Max | Min | Nom. | Max |
| A | 2.78 | 3.17 | 3.56 | 2.28 | 2.67 | 3.06 |
| A1 | 2.43 | 2.79 | 3.15 | 1.93 | 2.29 | 2.65 |
| b | 0.18 | 0.20 | 0.22 | 0.18 | 0.20 | 0.22 |
| c | 0.11 | 0.15 | 0.17 | 0.11 | 0.15 | 0.18 |
| D1/E1 | 28.96 | 29.21 | 29.46 | 35.64 | 36.00 | 36.36 |
| D2/E2 | 25.5 BSC | | | 31.5 BSC | | |
| e | 0.50 BSC | | | 0.50 BSC | | |
| F | 7.05 | 7.75 | 8.45 | 7.05 | 7.75 | 8.45 |
| H | 70.00 BSC | | | 70.00 BSC | | |
| K | 65.90 BSC | | | 65.90 BSC | | |
| L1 | 74.60 | 75.00 | 75.40 | 74.60 | 75.00 | 75.40 |

Note:

1. All dimensions are in inches except CQ208 and CQ256, which is in millimeters.
2. BSC equals Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.

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